1. INTRODUCTION
Increasing computational demand on mobile devices calls for energy-friendly solutions for accelerating single programs. In the multicore era, thread level parallelism (TLP) can accelerate single-threaded programs without requiring power-hungry cores. HELIX-RC, a recently proposed co-design between the HELIX parallelizing compiler and its target architecture, shows that substantial TLP can be extracted from loops with small bodies by optimizing core-to-core communication. Previously, the effectiveness of the HELIX-RC approach has been demonstrated through simulation. In this paper, we evaluate a HELIX-RC-like solution on a real platform.

We have developed a simplified version of the HELIX-RC architecture that we call unified cache, and we have implemented it on an FPGA board. Our design augments a multicore platform with a simplified ring cache—the architectural component of the HELIX-RC co-design. With the aid of microbenchmarks, our FPGA prototype confirms the HELIX-RC findings.

After describing both the ring cache and the parallel code generated by the HELIX compiler, we sketch the design of the unified cache and we evaluate its implementation on a Xilinx VC707 FPGA board.

2. BACKGROUND
The HELIX compiler automatically parallelizes sequential programs by distributing their loop iterations around a ring of cores. On conventional commodity platforms, dependences between loop iterations are satisfied through the memory hierarchy. The resulting high latency severely limits performance on such systems. In HELIX-RC, we proposed architectural support called ring cache to lower communication latency and enable more parallelization.

2.1 Helix Execution Model
HELIX [3, 4] accelerates programs by finding the most promising loops to parallelize. Successive iterations of each parallelized loop run on adjacent cores. For each data dependence between loop iterations, the compiler produces a sequential segment of code. The instances of a sequential segment running on separate cores must be executed in the same order as in the original sequential loop. So the compiler brackets each sequential segment with synchronization operations: signal ends the segment by signaling other cores that it has finished, and wait begins a segment by waiting for such a signal.

2.2 Conventional Inter-Core Communication
In commodity processors, cores communicate through memory. A core that needs data from another one uses the cache coherence protocol [5], which locates the data and moves it to the requesting core. Because coherence protocols are reactive, each request incurs a heavy overhead, on the order of a hundred cycles.

2.3 Ring Cache
To reduce communication latency between the cores of a conventional multicore processor, HELIX-RC [2] introduces ring cache: a light-weight architectural enhancement. HELIX-RC adds a ring node to each core and connects these nodes in a ring. When a ring node receives program data or synchronization signals, it passes them immediately to its successor node. This proactive communication around the ring of cores lowers latency and thereby enables loop parallelization that would otherwise be infeasible.

3. UNIFIED CACHE
To quantify the advantages of adding ring cache to a real platform, we implemented a simplification of it called unified cache.

3.1 Overview
Unified Cache is a customized shared cache in a chip multiprocessor. It has an input port from each core. During each sequential segment of a parallelized loop, a core uses this shared cache instead of its private first-level data cache (DL1). Code at the start of a parallelized loop primes the unified cache for the loop's sequential segments. Termination of the loop triggers a flush operation that writes unified cache data back to DL1.

3.2 Implementation
The unified cache handles core-to-core communication both for sharing data and synchronizing parallel execution.

Data. Data coming into the unified cache from cores enters queues that buffer and order the data by its core of origin. The queues are needed because the unified cache has a multiport RAM block that can perform multiple data reads, but only one write at a time. As the queues hold in-flight data, they are searched for every read request, which minimizes the delay between a store and a subsequent load.

Synchronization. Signals are connected to a bank called the signals bank, which performs n reads and n writes in a single cycle, where n is the number of input ports. This enables the
uniform cache to handle intensive synchronization requests from cores without stalls.

4. EXPERIMENT AND RESULTS
We implemented the uniform cache on a LEON3 platform. Our results reinforce those of the HELIX-RC simulations: Lowering core-to-core communication latency to fewer than 10 clock cycles enables parallelization of small loops that would otherwise be infeasible.

4.1 Platform
We synthesized our LEON3 [1] platform with the parameters shown in Table 1. Each core in the LEON3 CMP has its own DL1 cache. Because there is no last-level cache, cache coherence is maintained through the DDR3 RAM. When unified cache is not in use, cores are interconnected through a shared AMBA bus, where they snoop memory requests to maintain coherence.

4.2 Benchmarks
To quantify the effects of adding unified cache to the system, we created two benchmarks: LinkedList and SCAN. Each is implemented in three ways: as a sequential program and as parallelized in two ways. The first parallelization relies on traditional spin locks, based on load and store instructions. The second parallelization relies on unified cache. Performance of each parallelized version is normalized to the respective sequential version.

LinkedList. This benchmark traverses a linked list of elements. After accessing an element e in the list, the benchmark calls a function \( f(e) \) that takes \( n \) cycles, where \( n \) is passed as a parameter to the benchmark. This benchmark has one sequential segment, which implements retrieval of the current list link from a previous iteration. Its parallel segment is the computation of \( f(e) \). We sweep the ratio between the number of cycles required by the parallel segment and the number required by the sequential segment.

SCAN. The Scan benchmark [6] also traverses a linked list of elements \( e \), accumulating \( \sum f(e) \) and replacing each element in the list with the sum that its contribution produces. As a result, it has two sequential segments: retrieval of the current list link from a previous iteration, and reading and updating the accumulator.

4.3 Results
Characterization. Adding the unified cache to the platform requires the modification of two crucial paths in the processor: memory operations and exception handling. Therefore, adding the unified cache might degrade platform frequency and add area and routing overhead. After synthesizing the system, we found that the addition of the unified cache did not incur a heavy penalty. Moreover, unified cache lowers the communication latency between cores from 58 cycles to 3 cycles. (Three cycles is the ISA defined minimum for one load and one store \([7]\).)

Finally, as incoming data to the unified cache is being queued, we expect store instructions to take longer than the two cycles that the ISA specifies \([7]\). Our measurements show that even in the worst case, when the queues for every port are fully utilized, store latency increases to only 4 cycles.

Unified cache increases parallelism. To show the importance of low-latency communication between cores, we ran the LinkedList benchmark on our platform sweeping parallel-to-serial ratio from 1× to 30× (Figure 2). As shown in this figure, unified cache soon outstrips the traditional spin lock solution. Therefore, unified cache allows parallelization of small loops that tend to have small parallel-to-serial ratios.

Testing Scan leads to the same conclusion as for LinkedList. We compiled Scan with 6 different functions \( f(e) \). Figure 3 shows that, compared to traditional spin locks, the unified cache helps parallelized Scan achieve higher performance with minimal \( f(e) \). Scan’s spin lock version struggles to improve performance even when compared to the spin-lock version of LinkedList. Hence, even for Scan, proactive inter-core communication is essential for accelerating the performance of small loops through parallelization.

---

**Table 1: LEON3 platform configuration.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Platform</td>
<td>LEON3</td>
</tr>
<tr>
<td>ISA</td>
<td>SPARC-v8c</td>
</tr>
<tr>
<td>Number of Cores</td>
<td>4</td>
</tr>
<tr>
<td>Cache Configuration</td>
<td>16 kByte, 4 ways</td>
</tr>
<tr>
<td>TLB Entries</td>
<td>16 Entries</td>
</tr>
<tr>
<td>FPGA Platform</td>
<td>Xilinx VC707</td>
</tr>
<tr>
<td>Main Memory</td>
<td>1GByte DDR3-RAM</td>
</tr>
<tr>
<td>Operating System</td>
<td>GNU/Linux 2.6.8</td>
</tr>
<tr>
<td>Number of Unified Cache Ports</td>
<td>4</td>
</tr>
<tr>
<td>Size of Unified Cache Queues</td>
<td>1 Entry</td>
</tr>
<tr>
<td>Unified Cache Signal Banks</td>
<td>64 Signals</td>
</tr>
<tr>
<td>Unified Cache Data Cache</td>
<td>4 kByte, 1 way</td>
</tr>
</tbody>
</table>
5. REFERENCES


