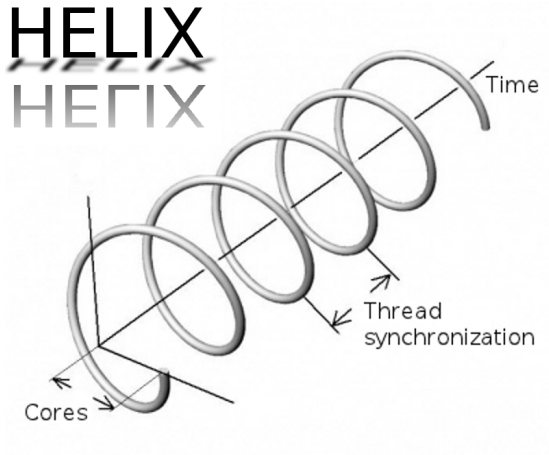
HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing

Simone Campanoni, Timothy M. Jones, Glenn Holloway
Vijay Janapa Reddi, Gu-Yeon Wei, David Brooks



Summary

- Motivation
- A simple idea
- Single loop parallelization
- Loop selection
- Evaluation
- Conclusion

Extraction of Thread-Level-Parallelism (TLP)

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- In multicore era: $\Uparrow$ performance $\Leftrightarrow$ TLP $\Uparrow$

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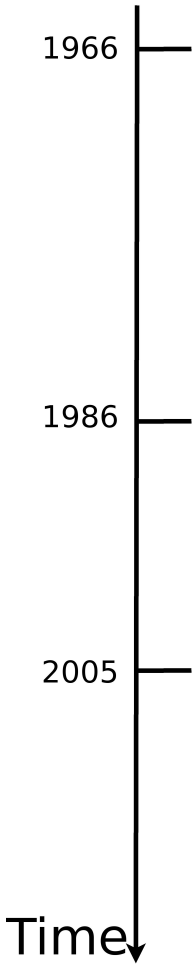

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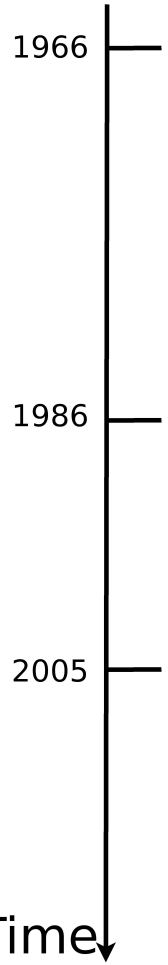

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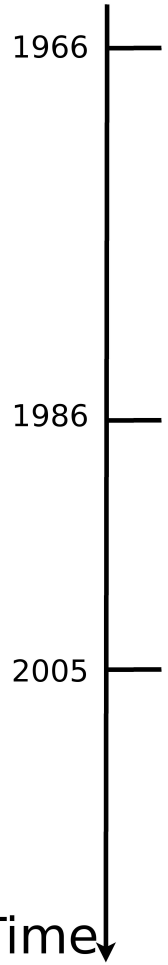

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Inter-core communication $\Rightarrow$ private cache access hit

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- General purpose technique
- Predictable speedup
  - Avoid slowdown
- $|\text{threads}| \leq |\text{loop iterations}|$

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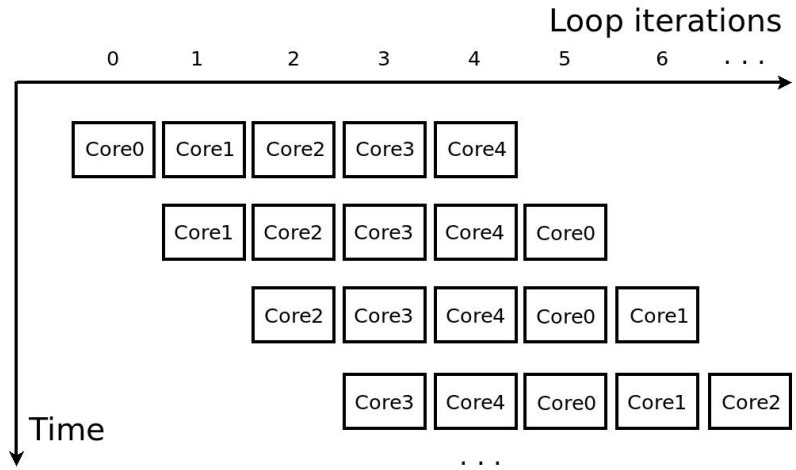

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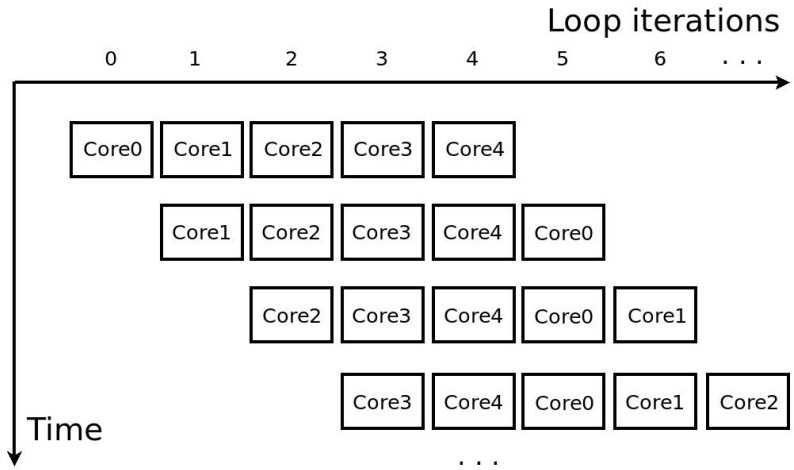

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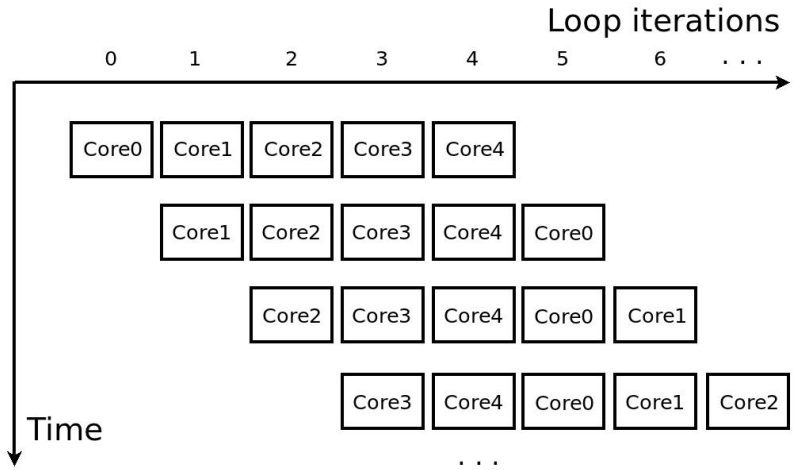

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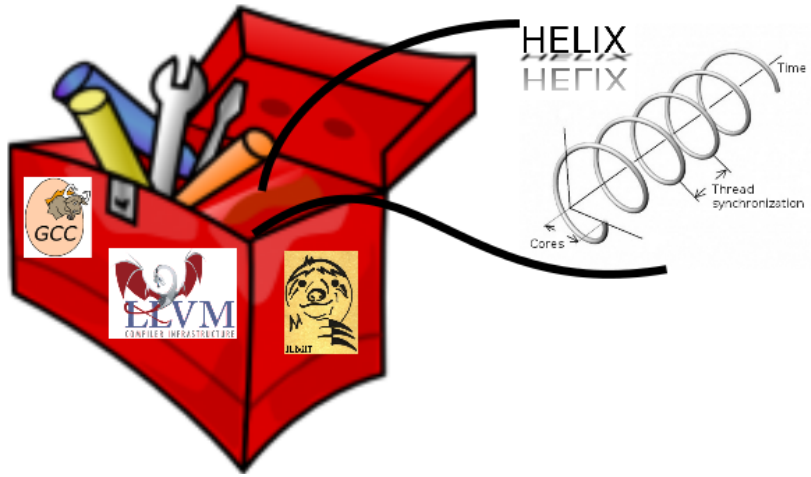

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A Simple Idea

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for (...){
    1: a = update(a);
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    3: b = update(b);
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- A simple program

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- Loop-carried data dependences 

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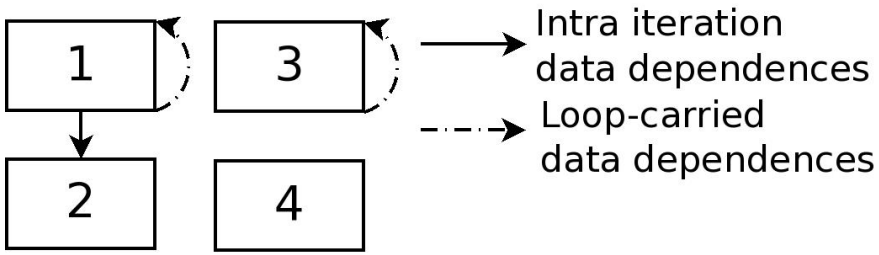

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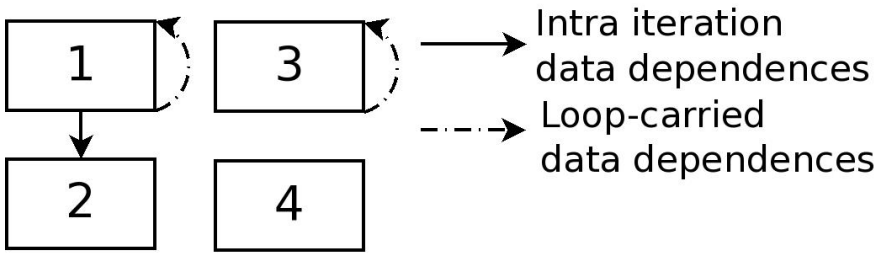

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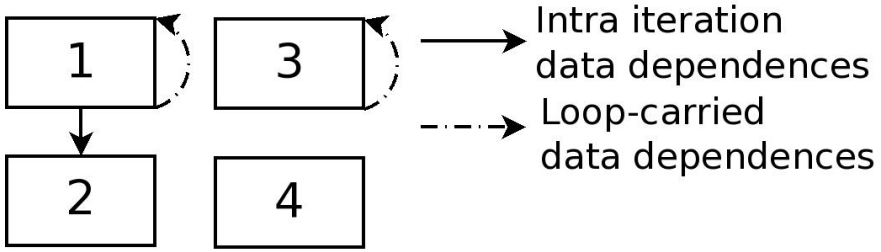

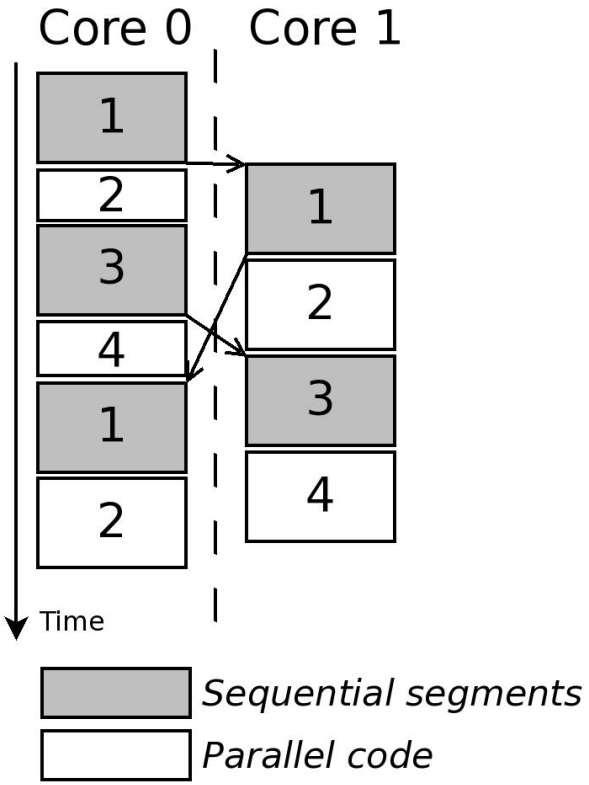

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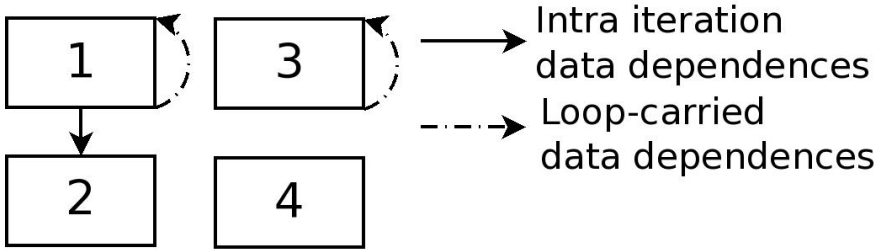

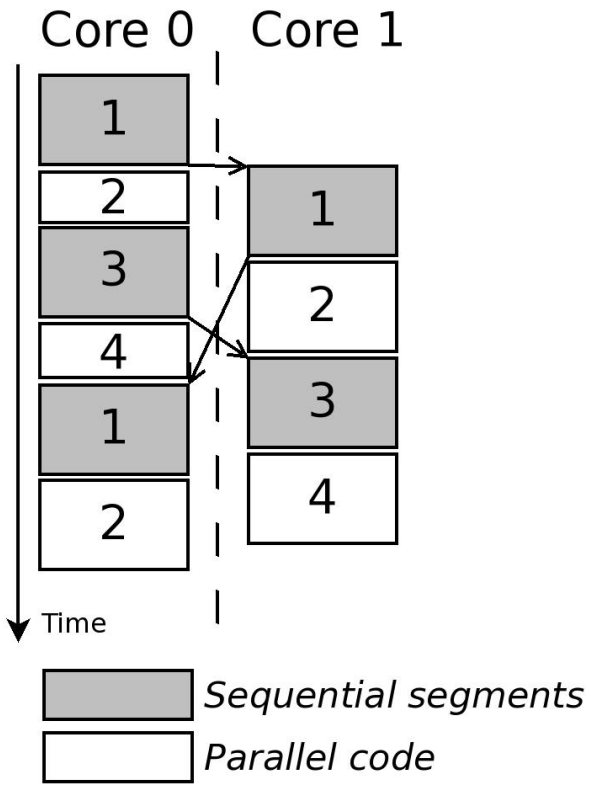

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Problem: amount of synchronization required increases drastically!

Overhead

Optimizations

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Notify threads

Adopted solutions

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  - Each loop uses all cores decided at compile time

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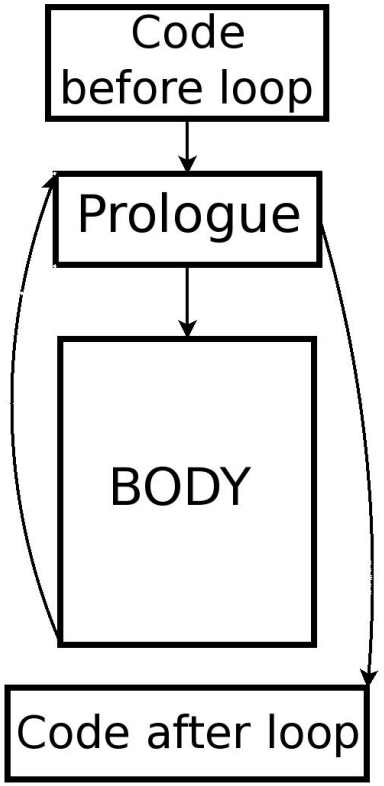

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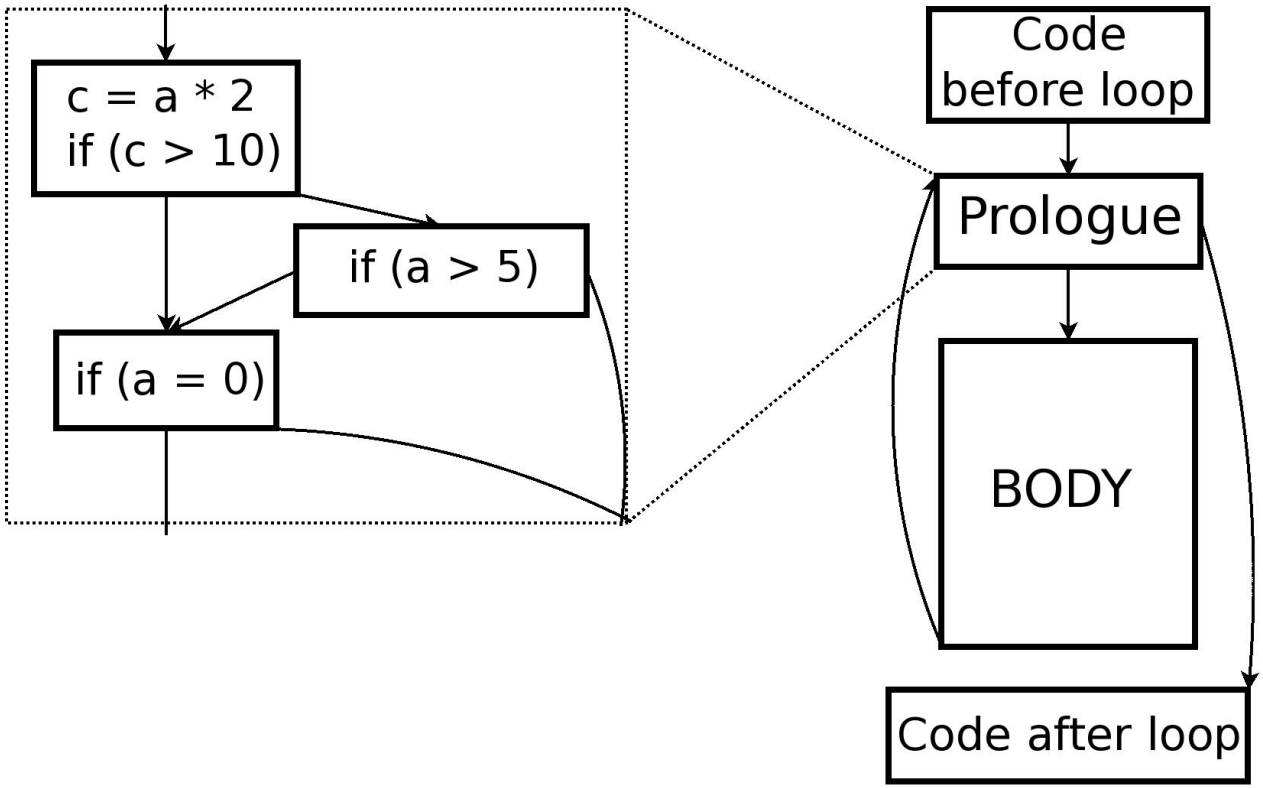

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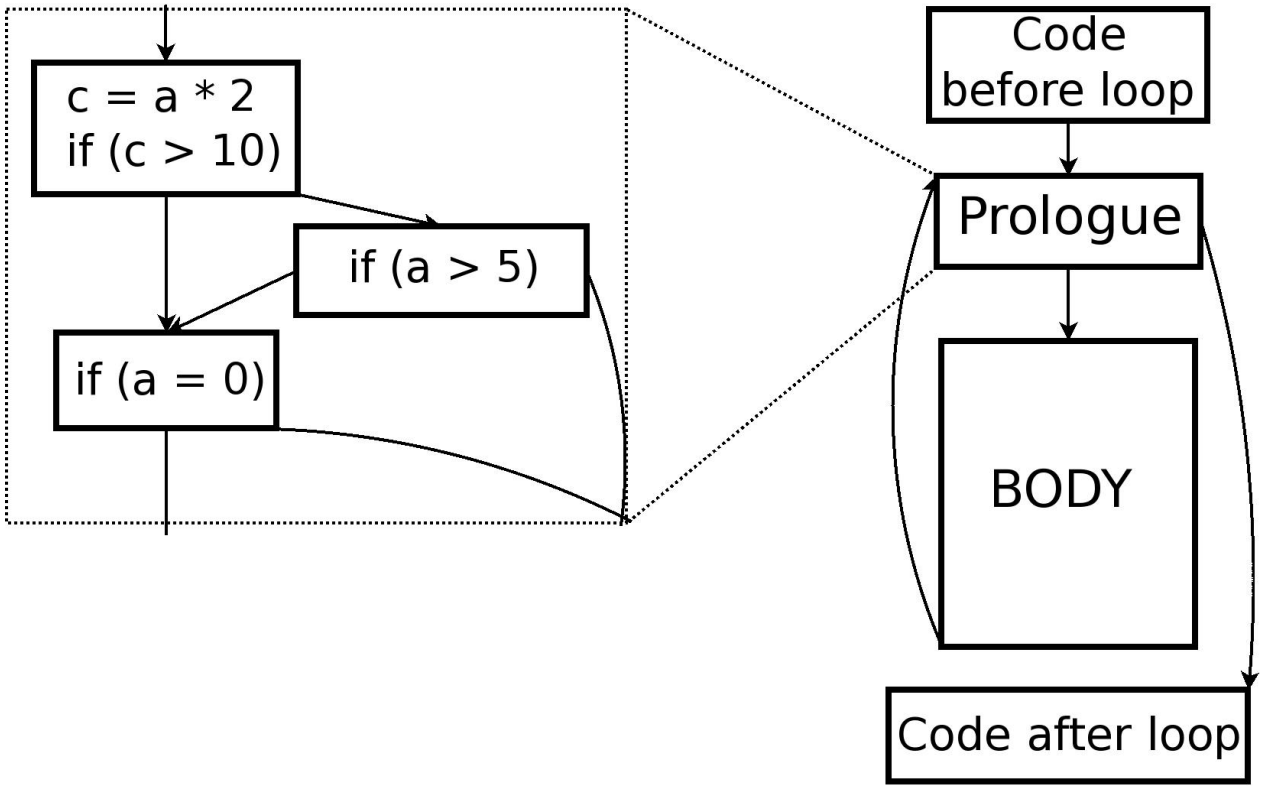

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- Best case: single exit controlled by an induction variable

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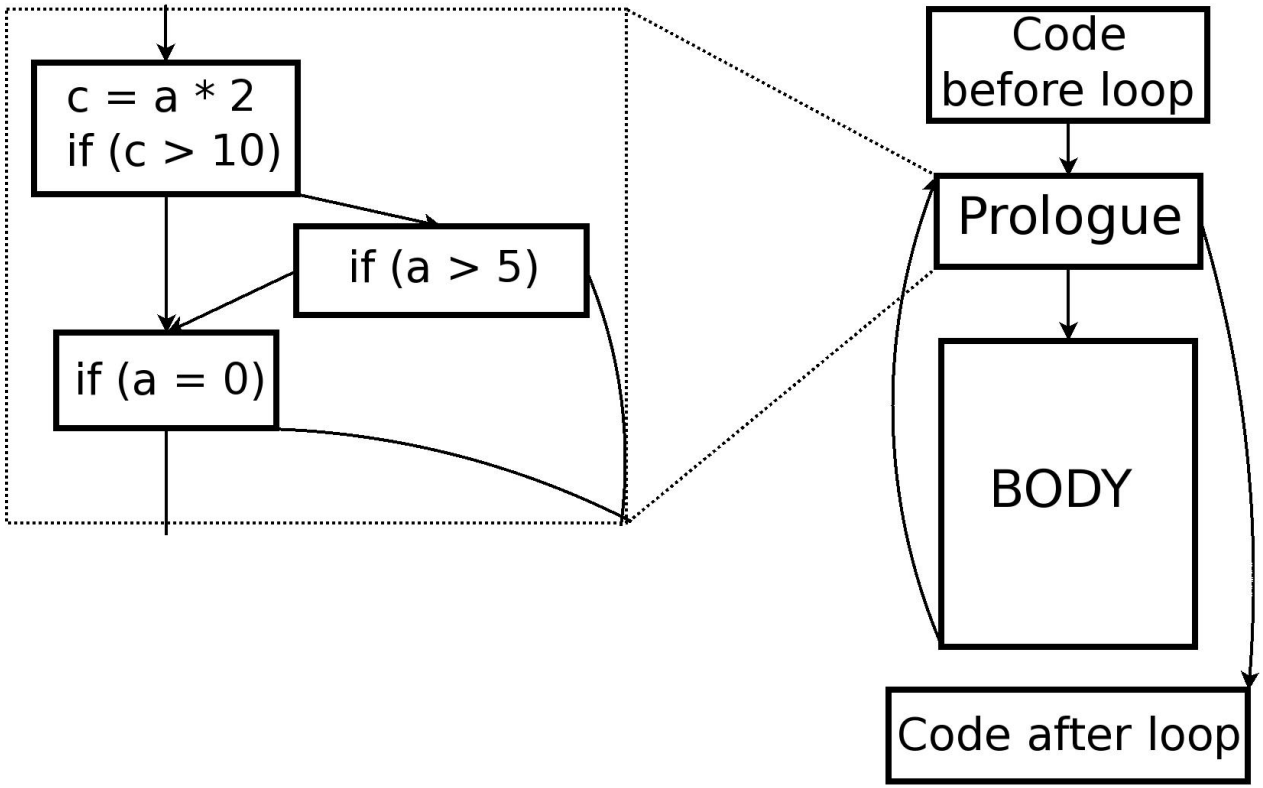

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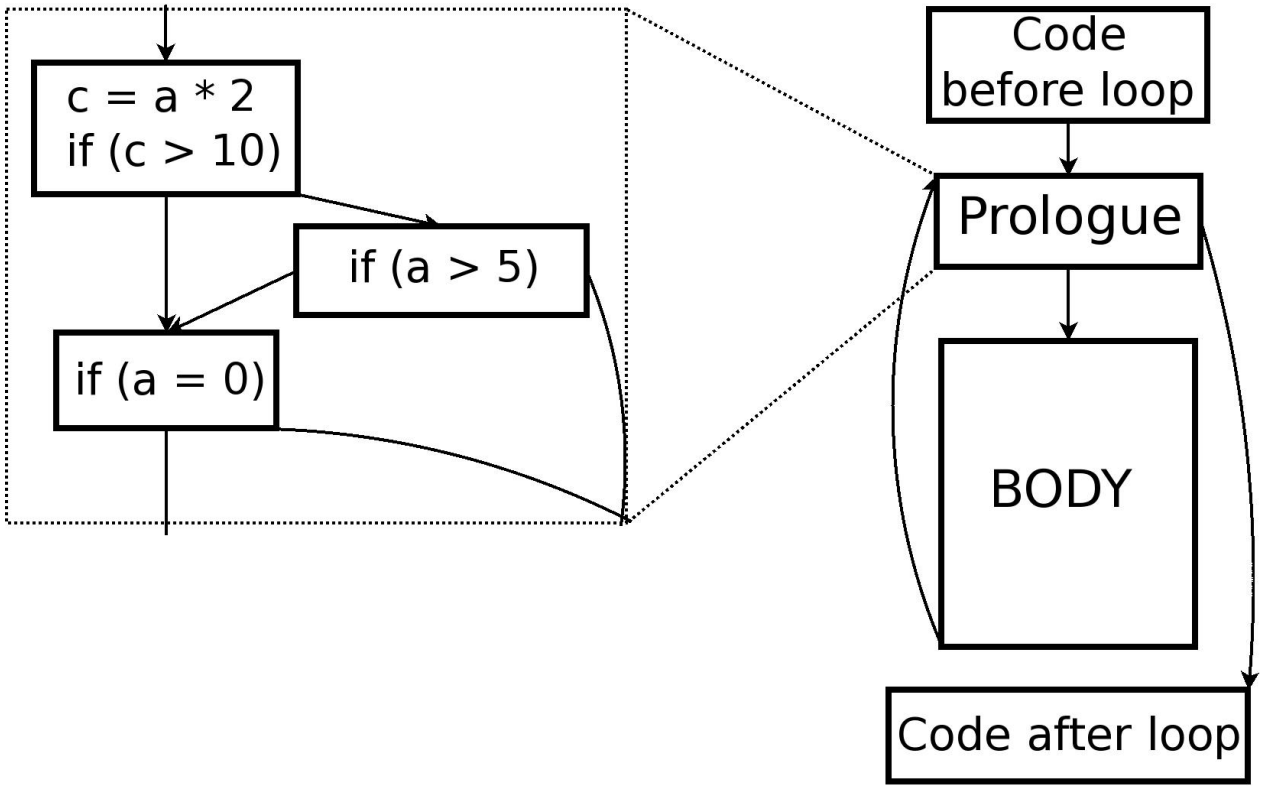

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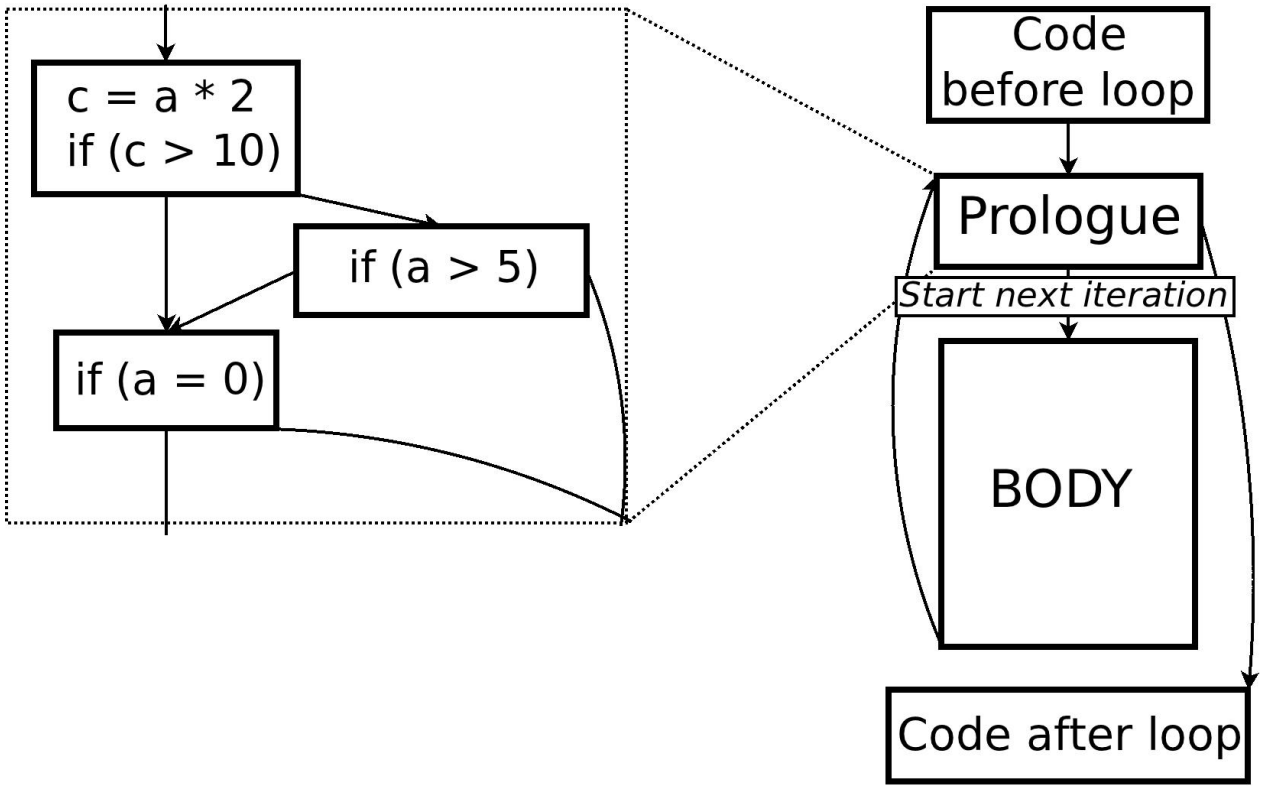

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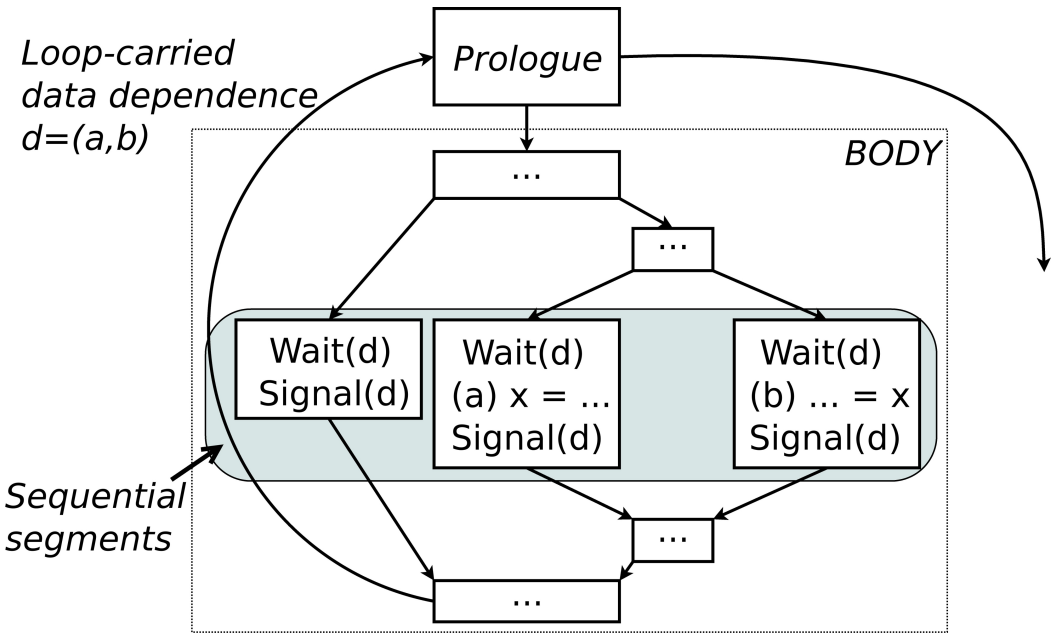

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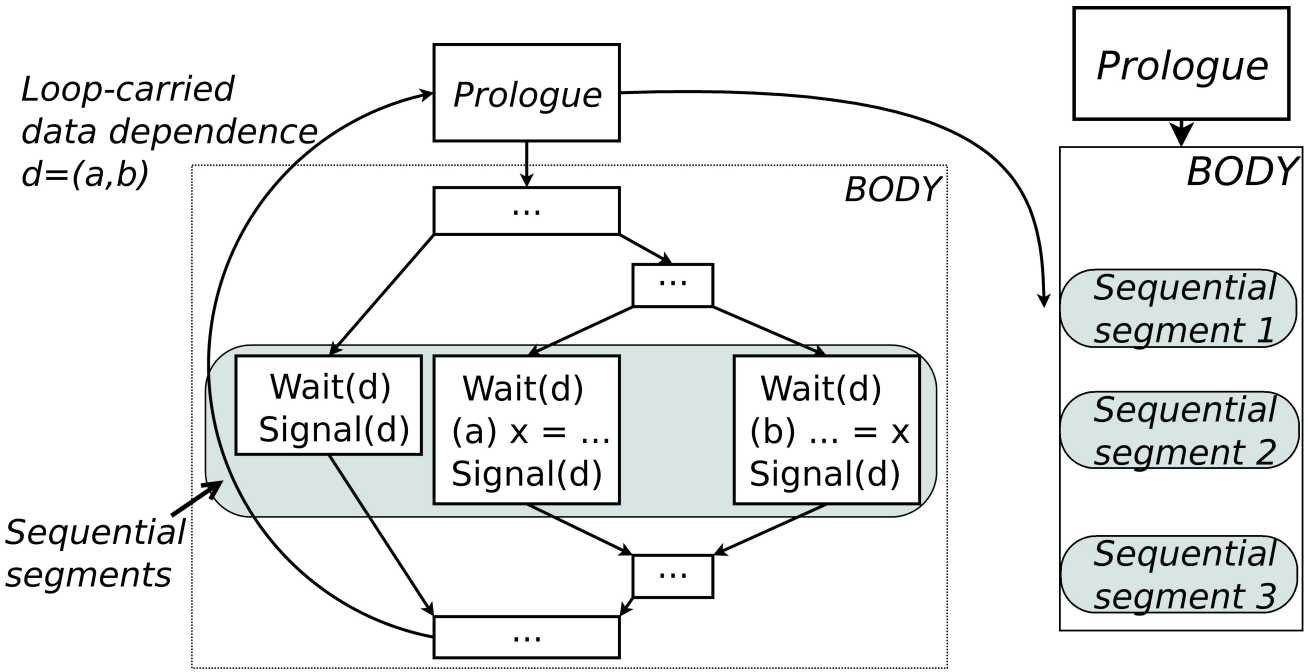

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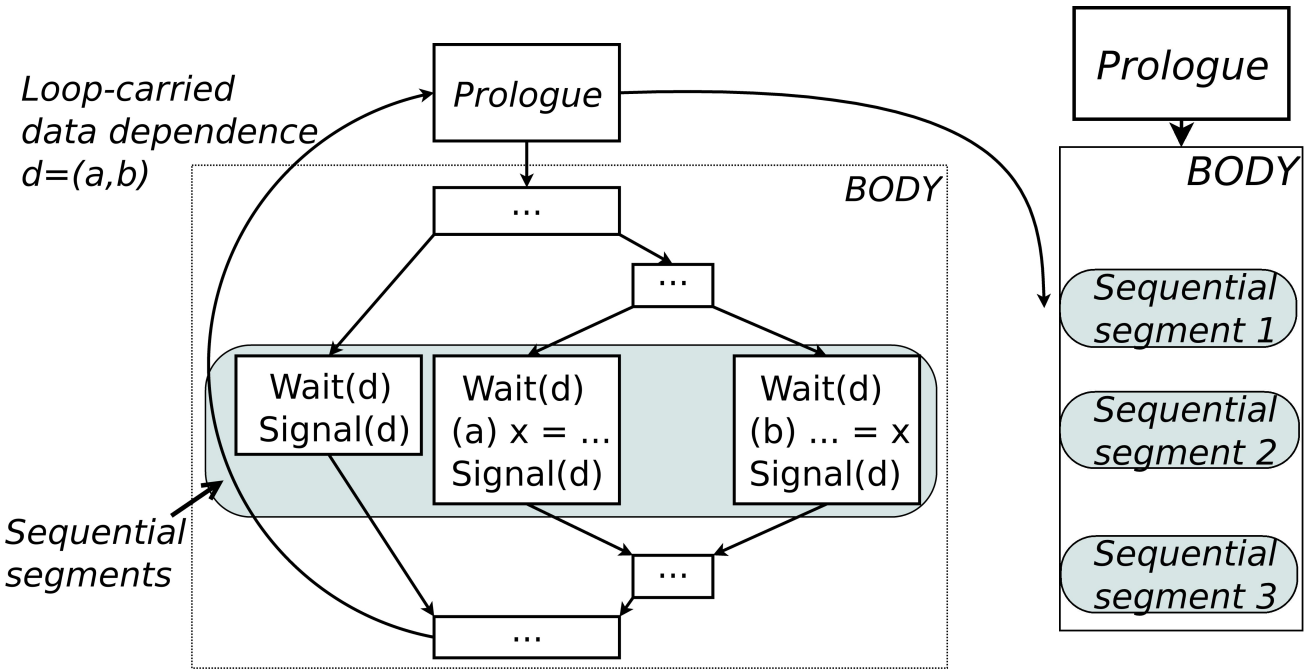
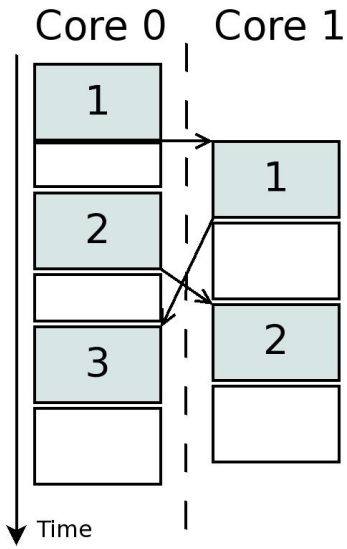
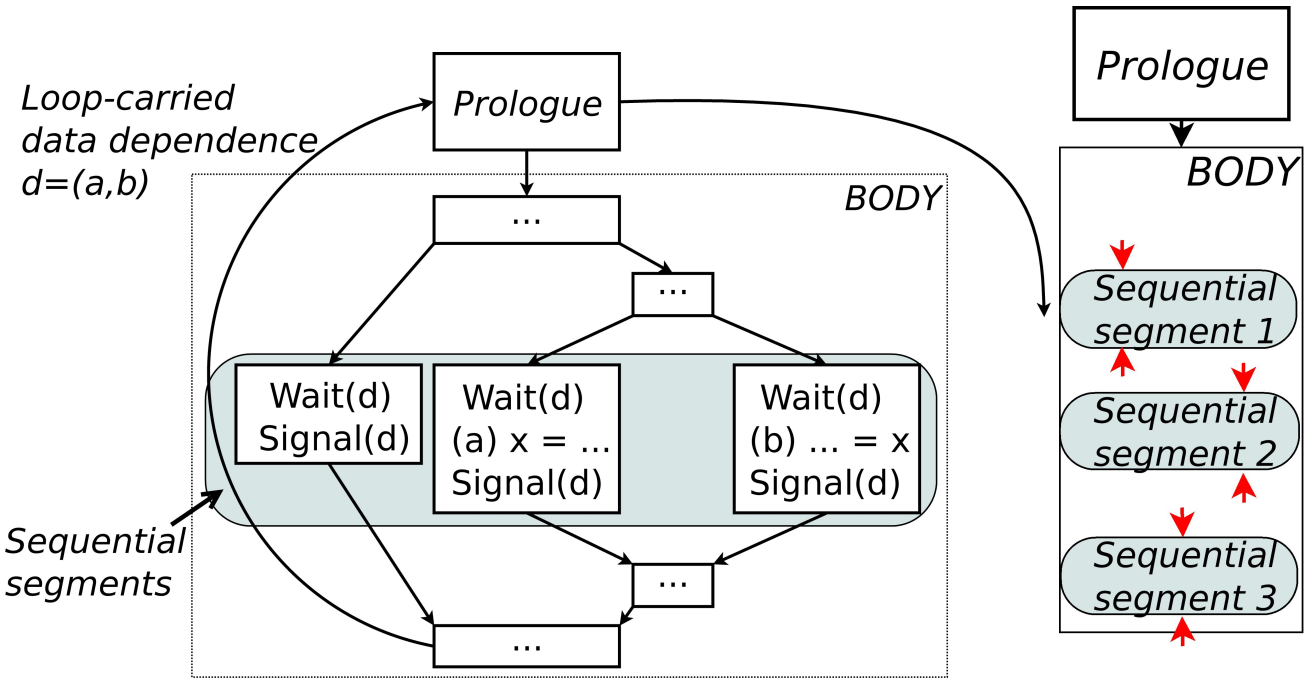


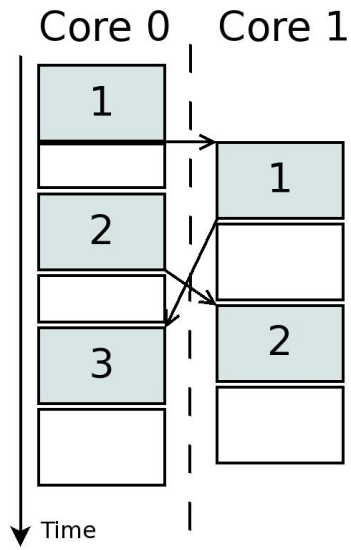


TLP among segments

Step 5: Minimizing Sequential Segments

Method inlining and code scheduling applied





TLP among segments

Steps 6 and 7

Step 6: Minimizing Signals

New analysis developed to minimize redundancy of signals

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New analysis developed to minimize redundancy of signals

- intra- and inter-data dependences

Theorem

Let $G = (N, E)$ be a data dependence redundance graph and let $N_{to\text{-}synch} \subseteq N$ be the set of dependences that includes every node without incoming edges and one node per cycle of G. Synchronizing the set $N_{to\text{-}synch}$ synchronizes the entire set of dependences N.

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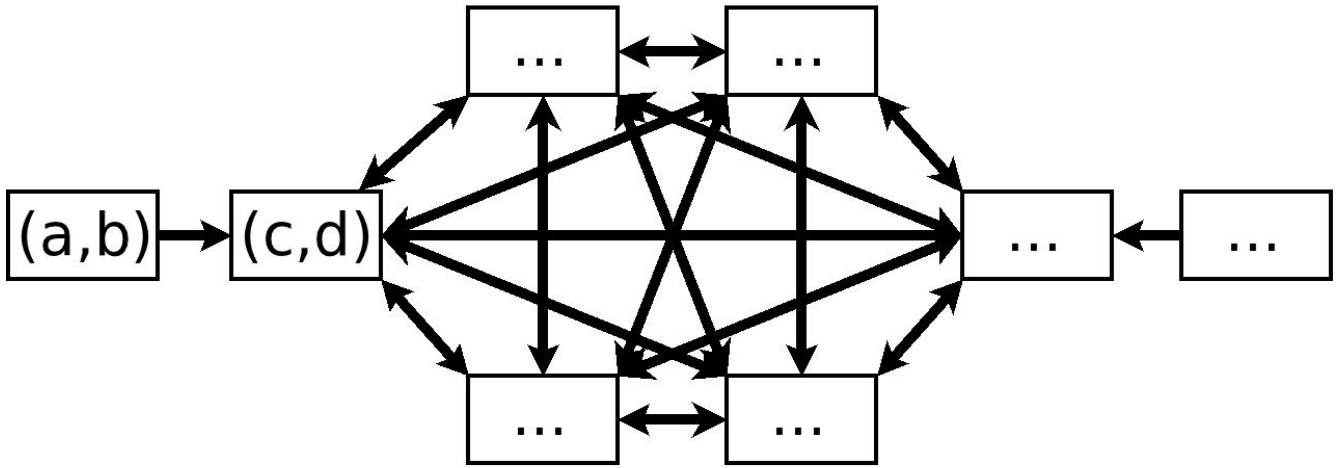

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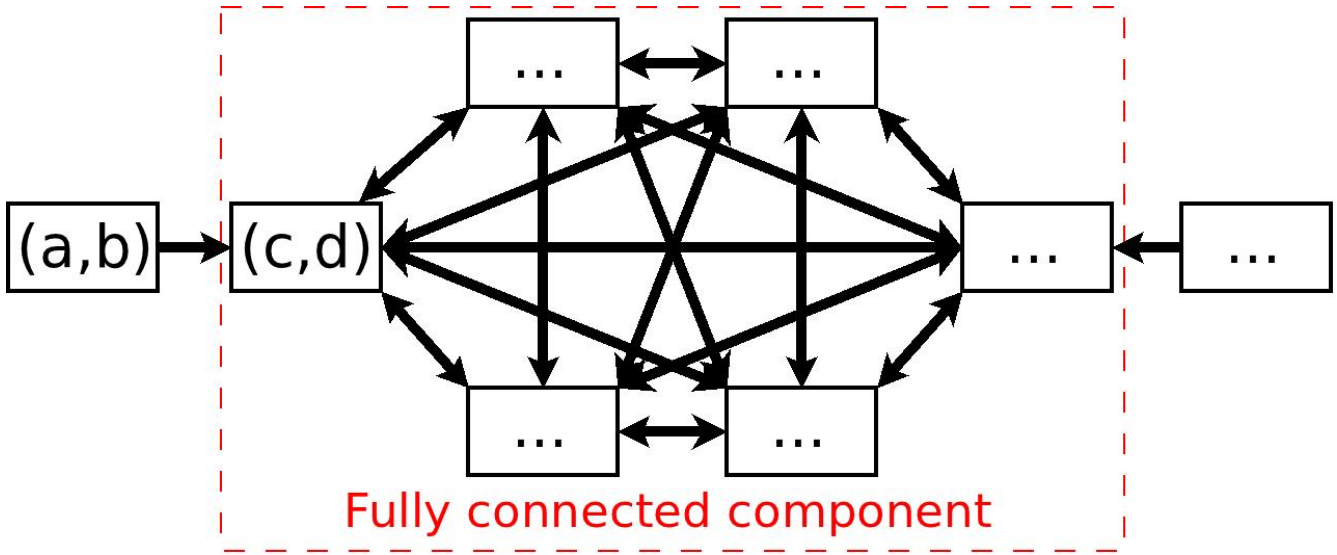

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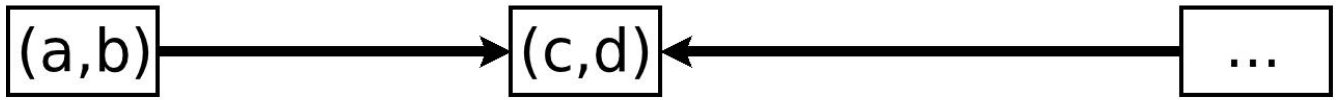

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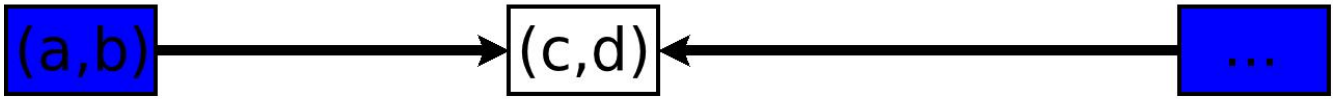

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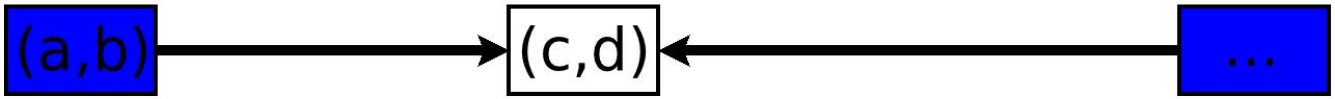

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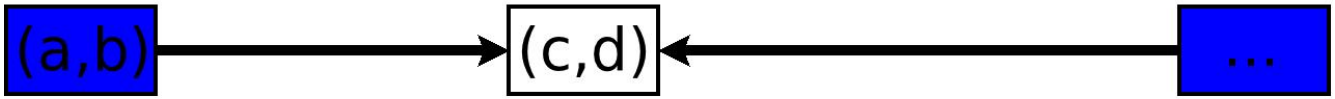

Step 7: Inserting Inter-Thread Communication

New analysis to minimize loads and stores of shared locations

Step 8: Coupling with Helper Threads

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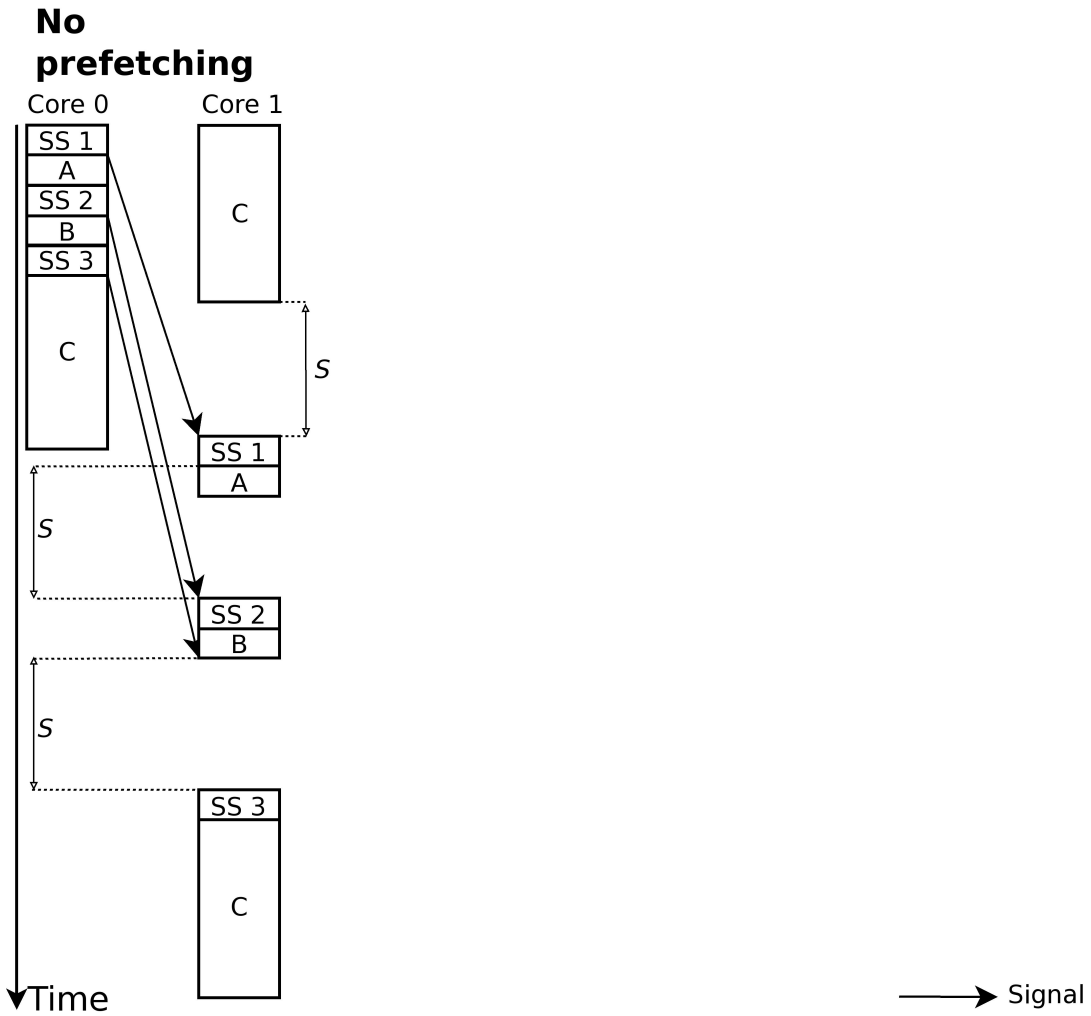

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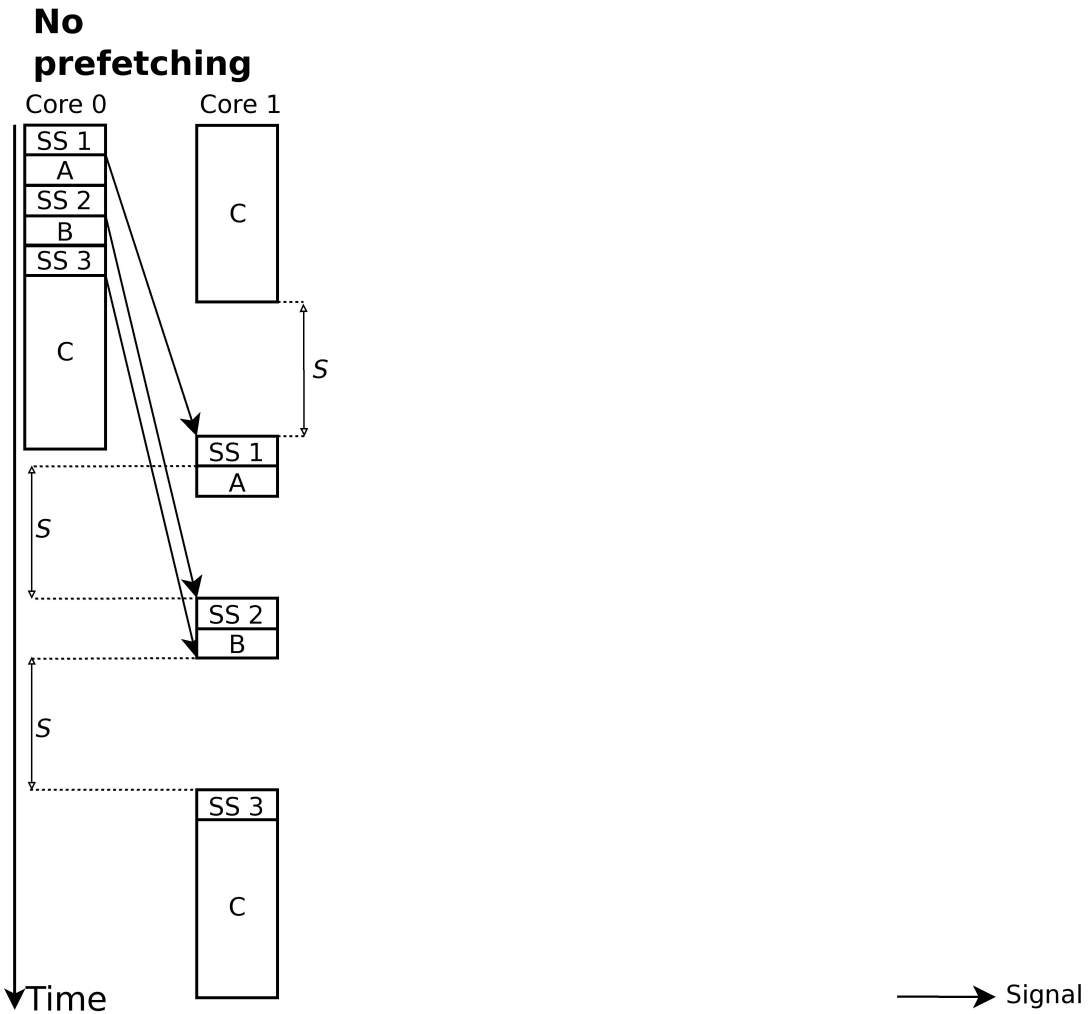

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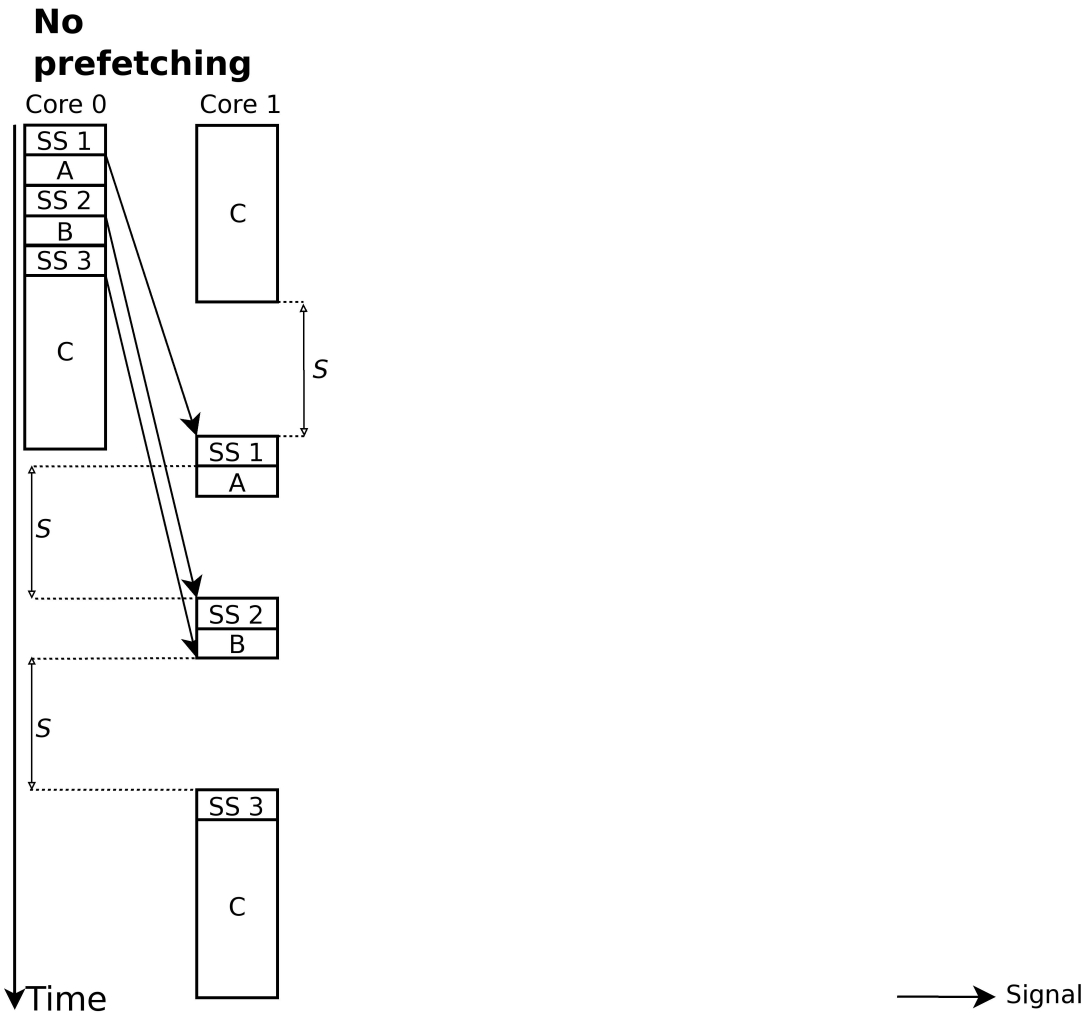

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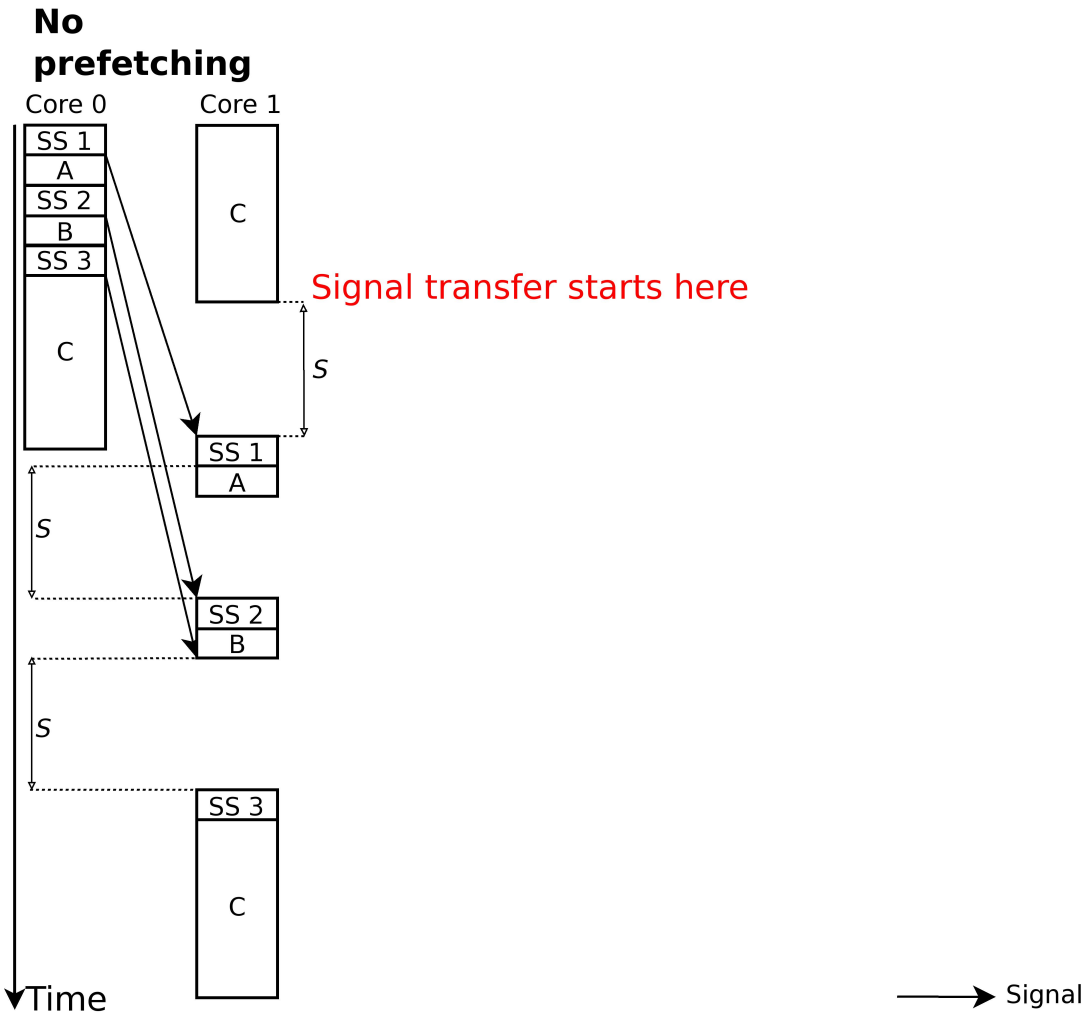

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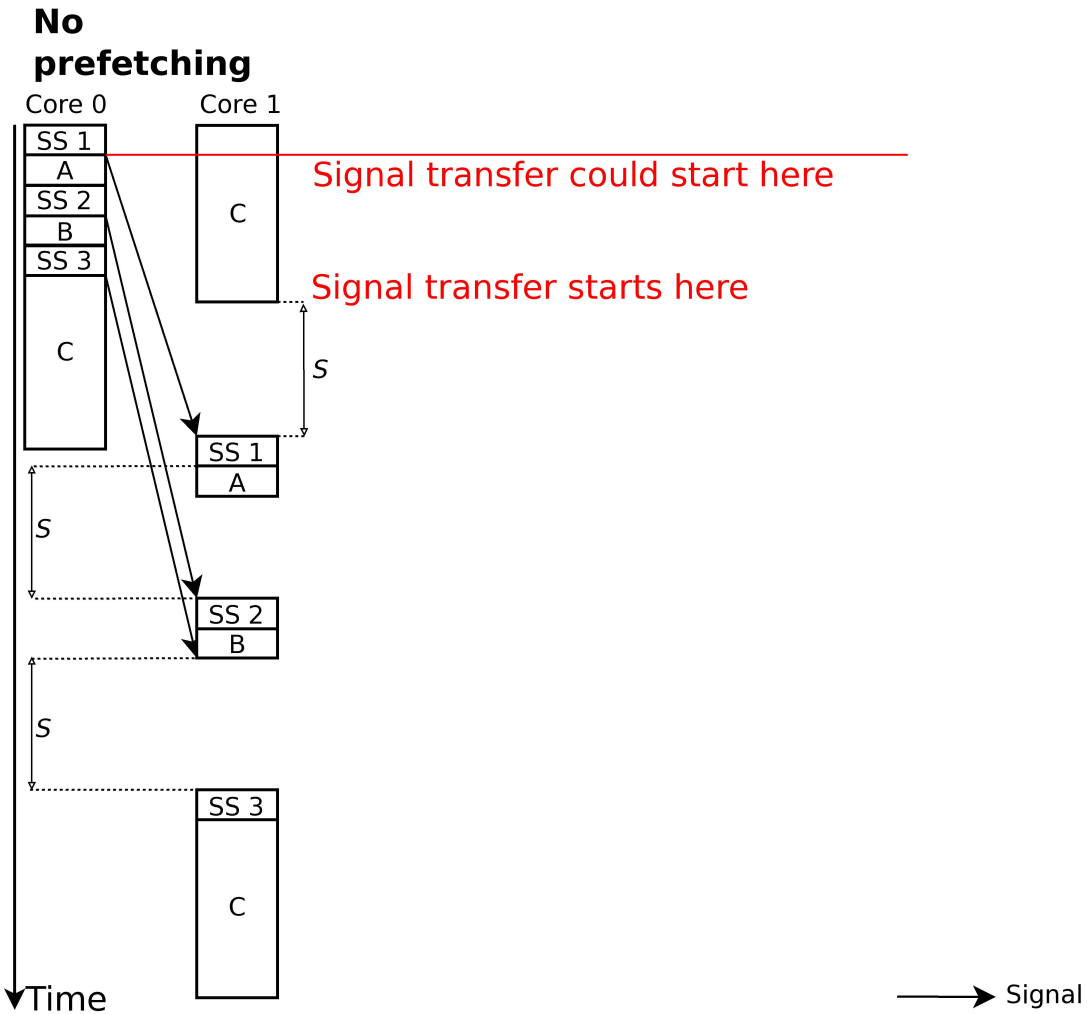

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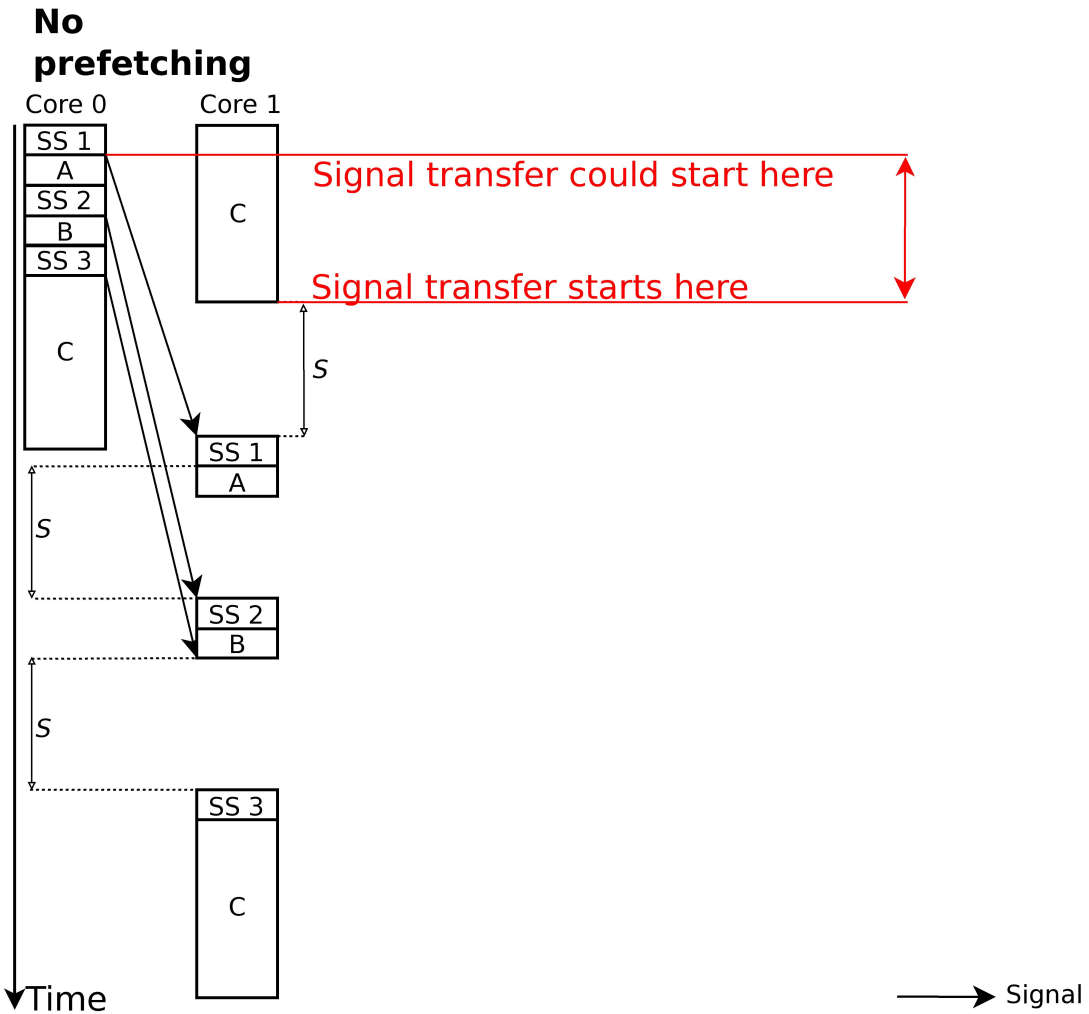

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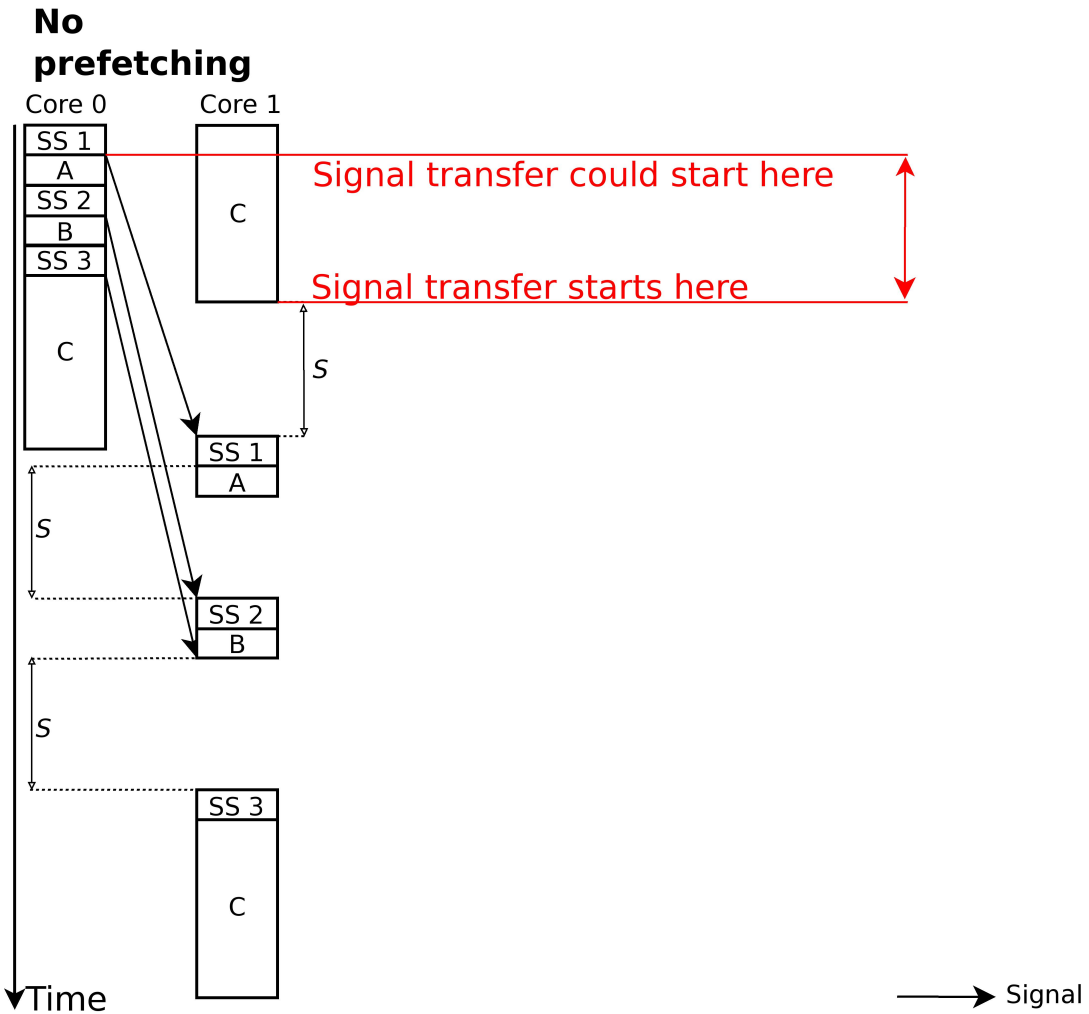

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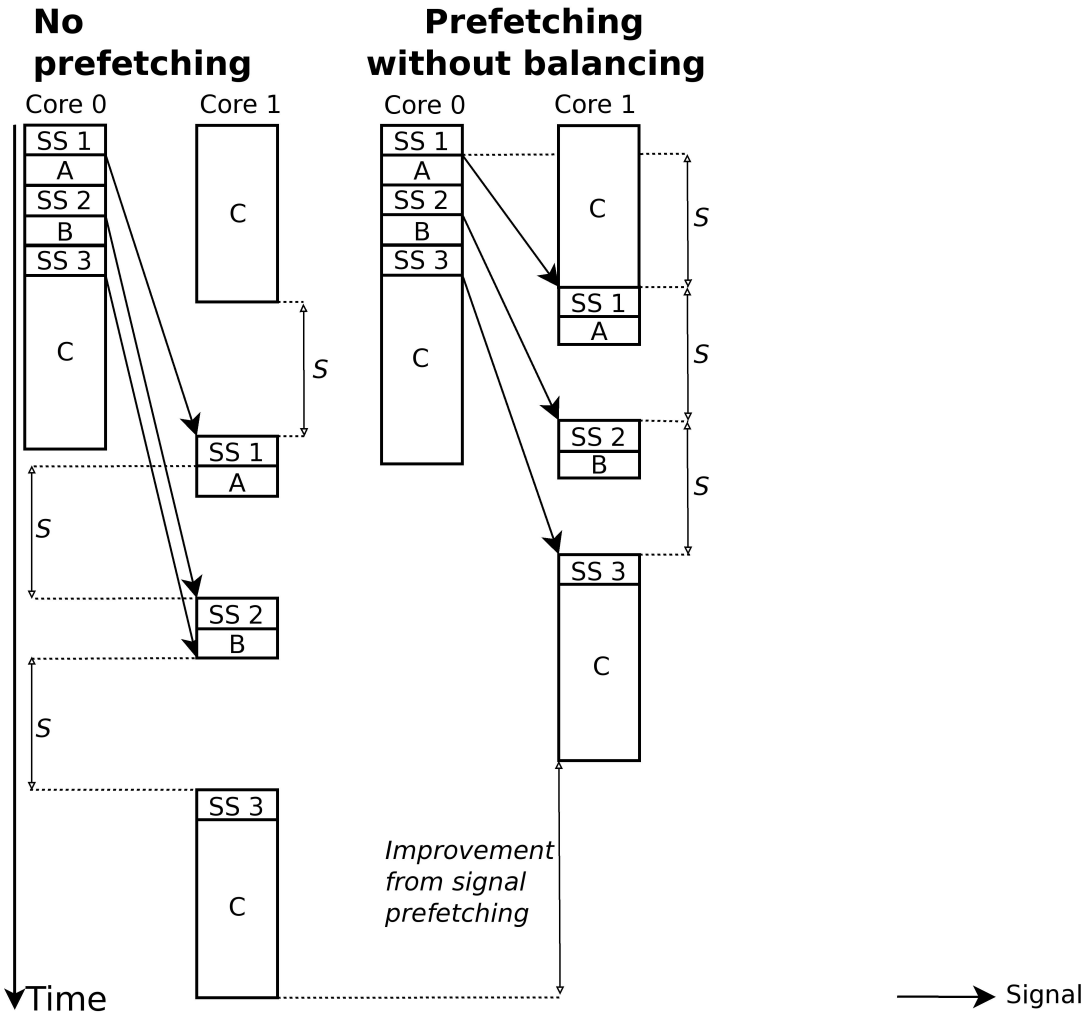

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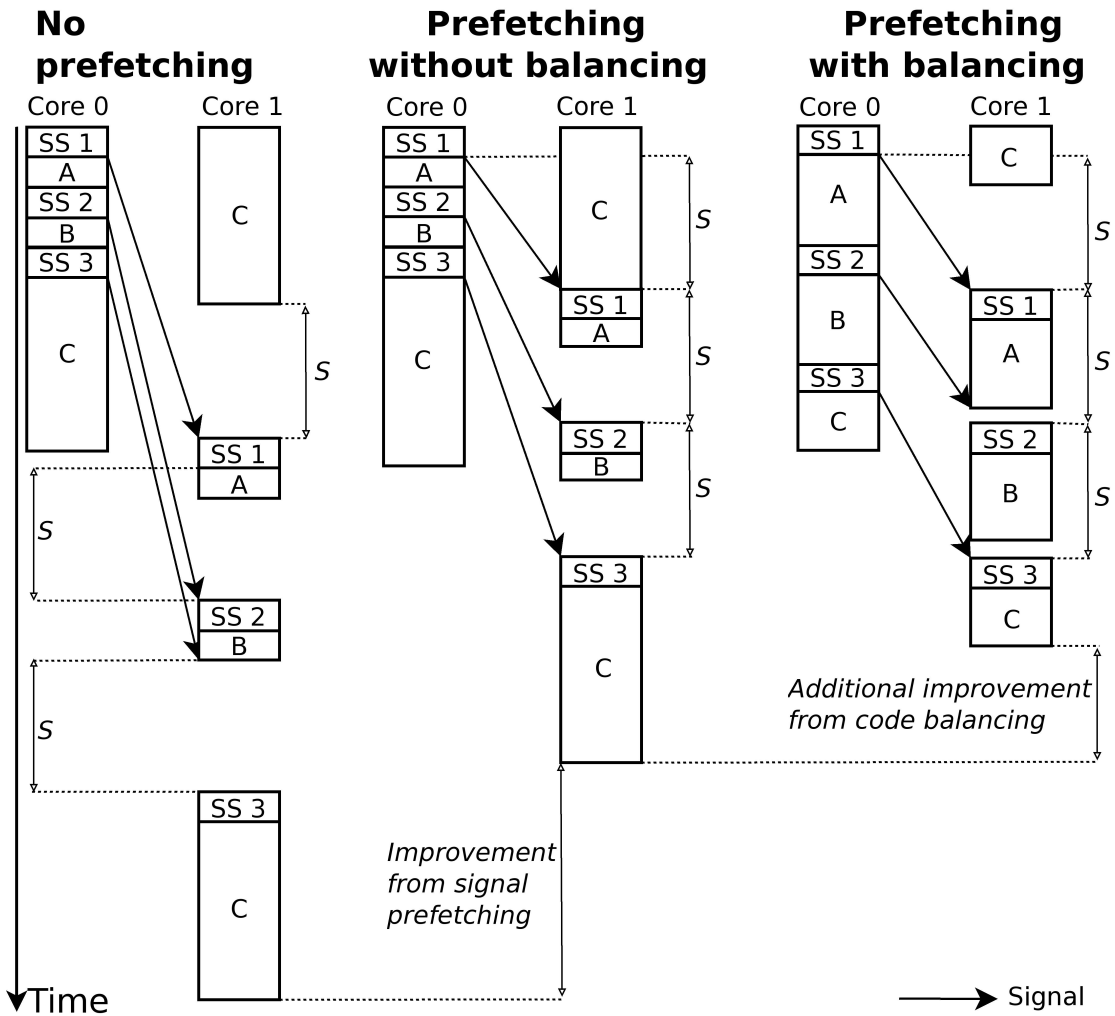

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- Evaluation
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HELIX approach

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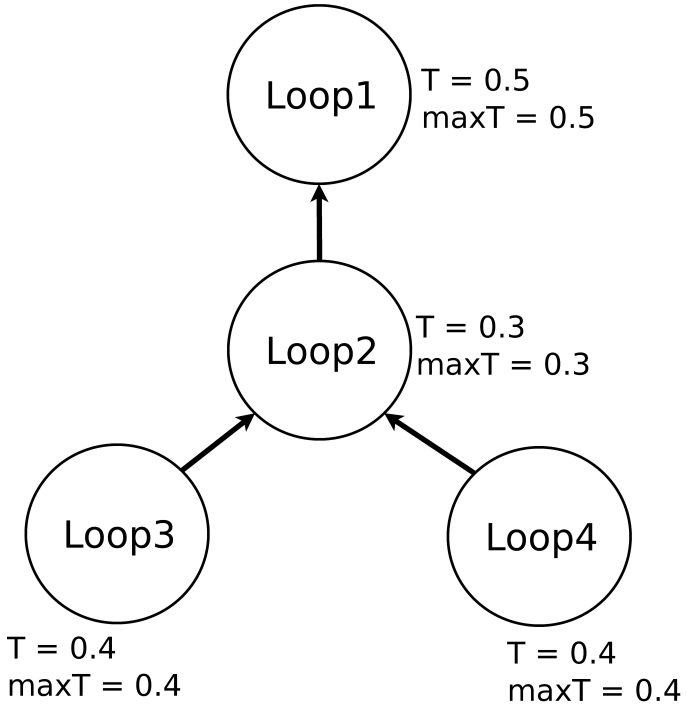
Thanks to characteristic of the produced code:

$$Sig = |\text{loop iterations}| \times |\text{sequential segments}|$$

Identify loops to parallelize

Propagate parallel code information



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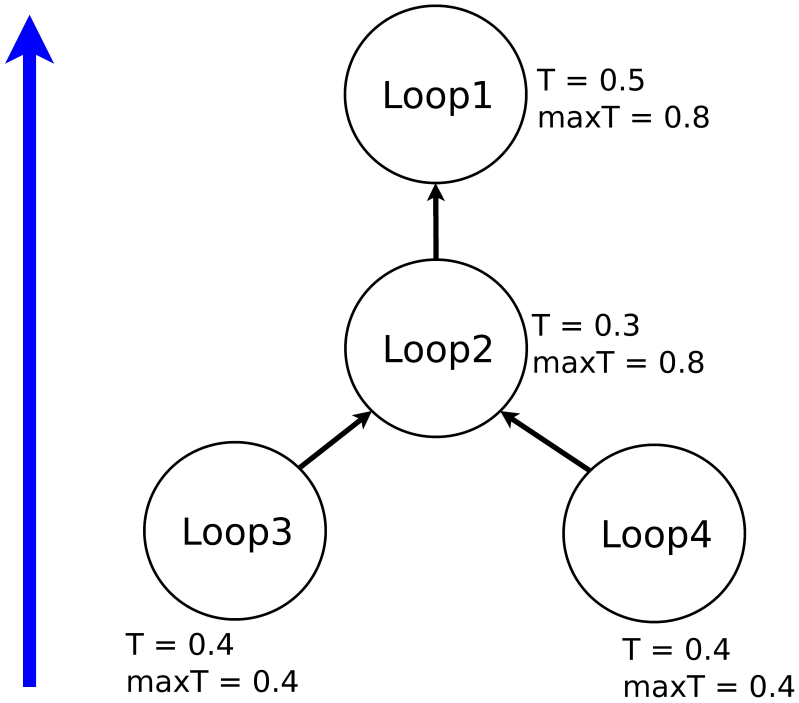

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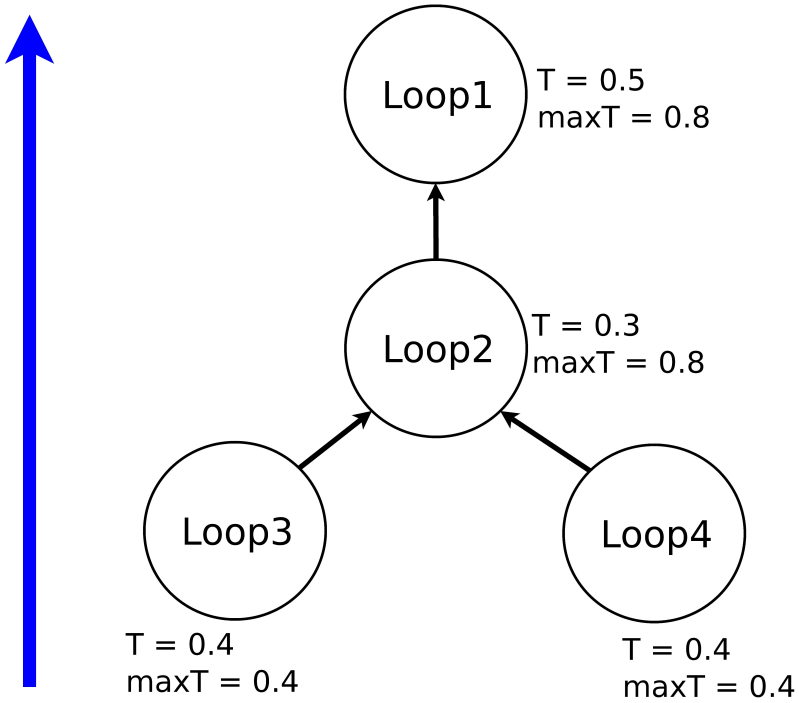

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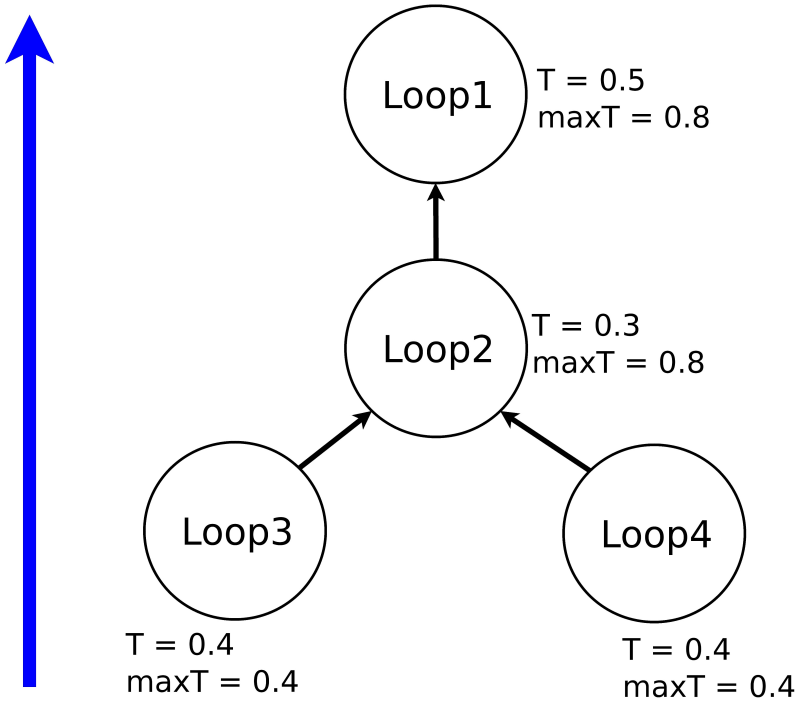

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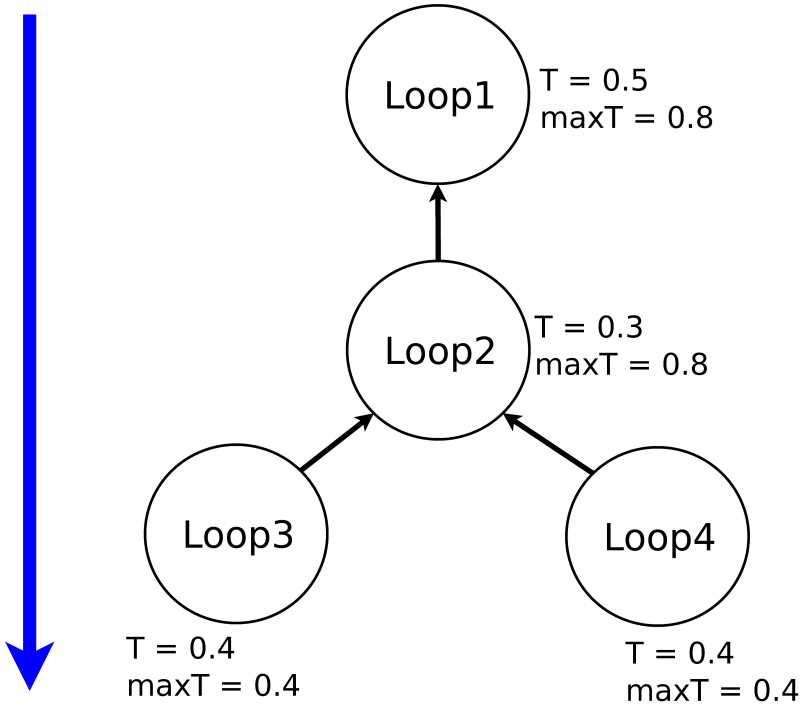

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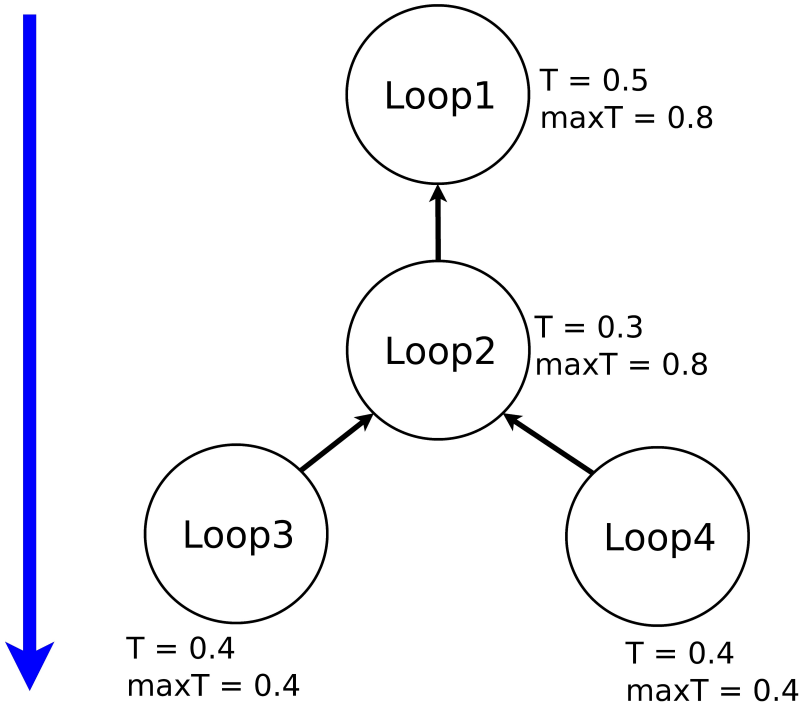

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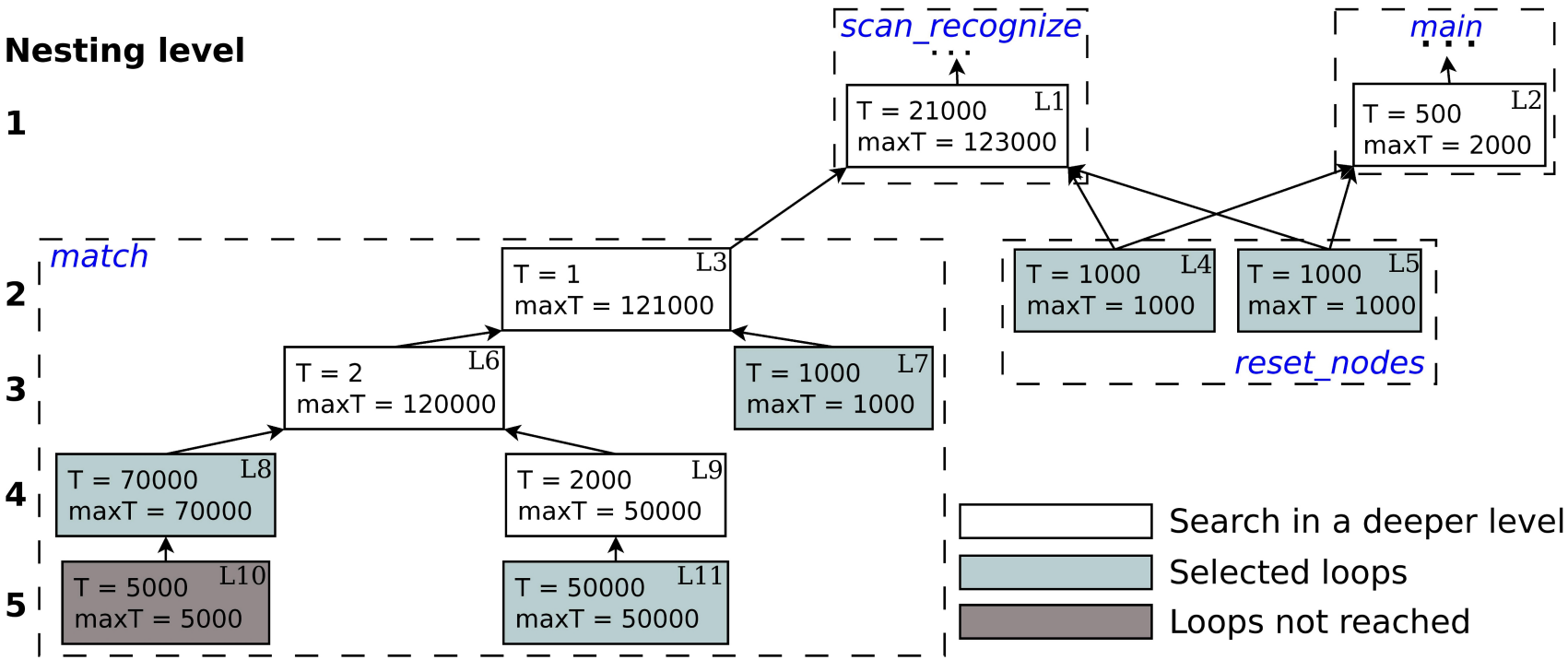
Is this an heuristic?

Loop Selection for 179.art



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- The input *train* is used to select loops
- The input *ref* is used to compute the speedups

Speedup Obtained on a Real System

Overall program speedup

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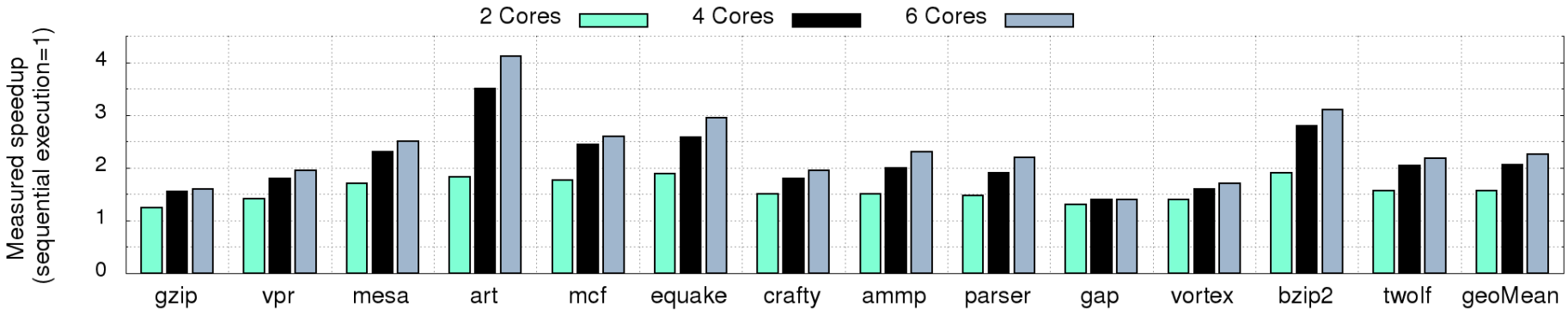

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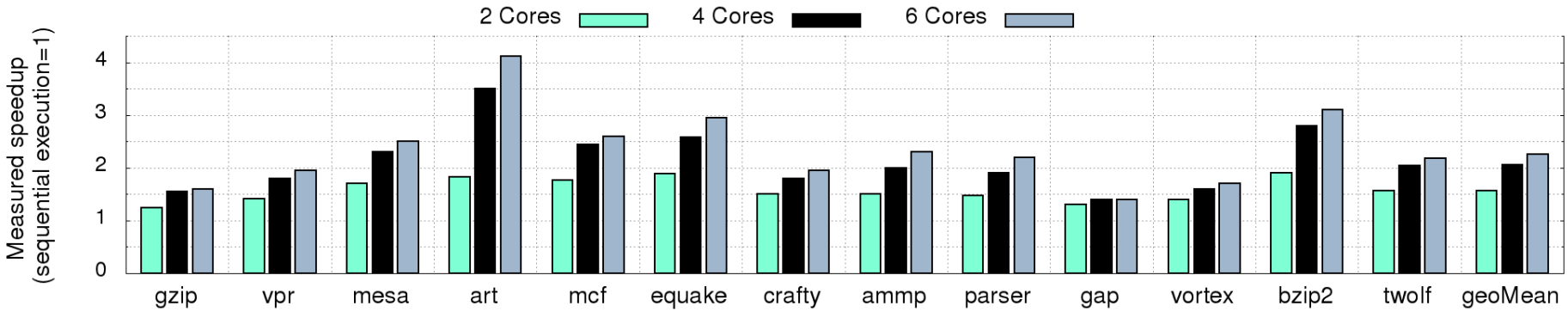

Most significant contributions

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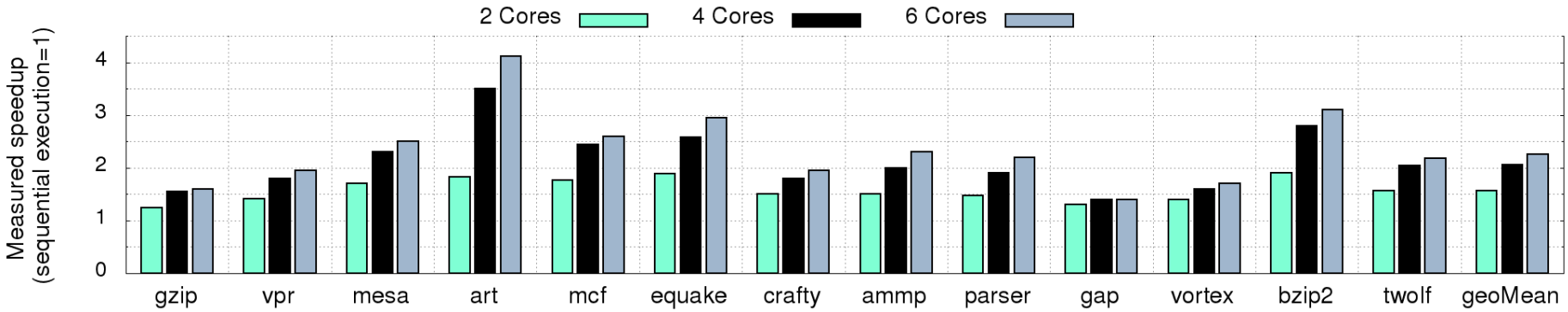

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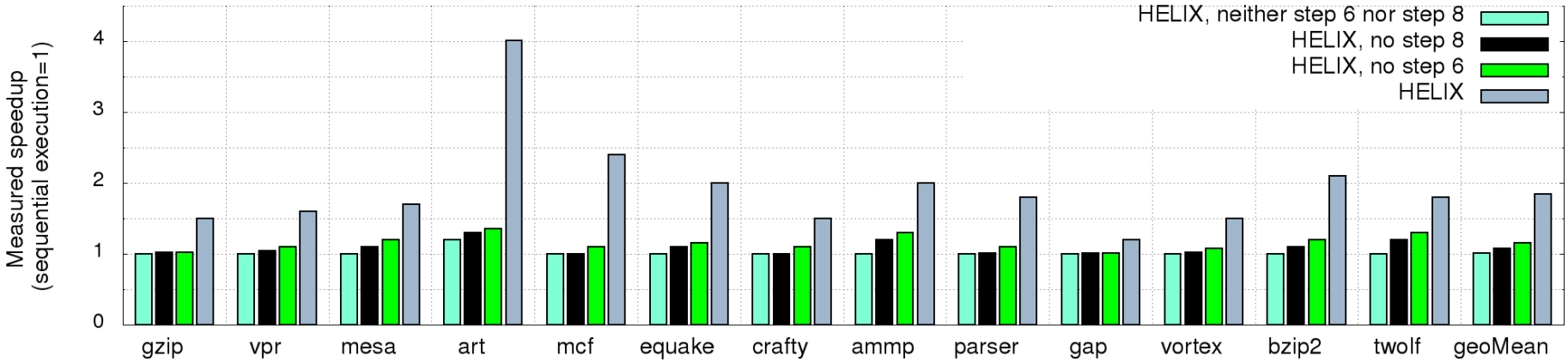

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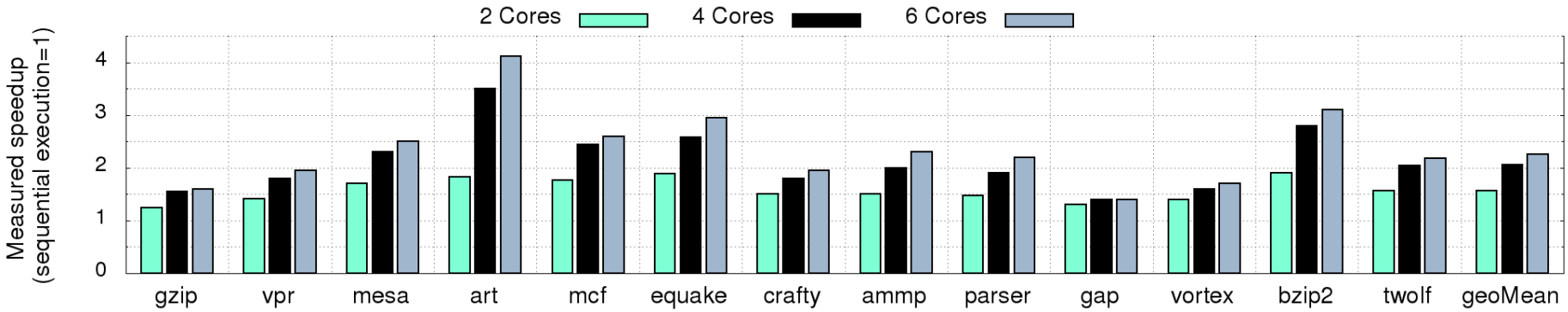

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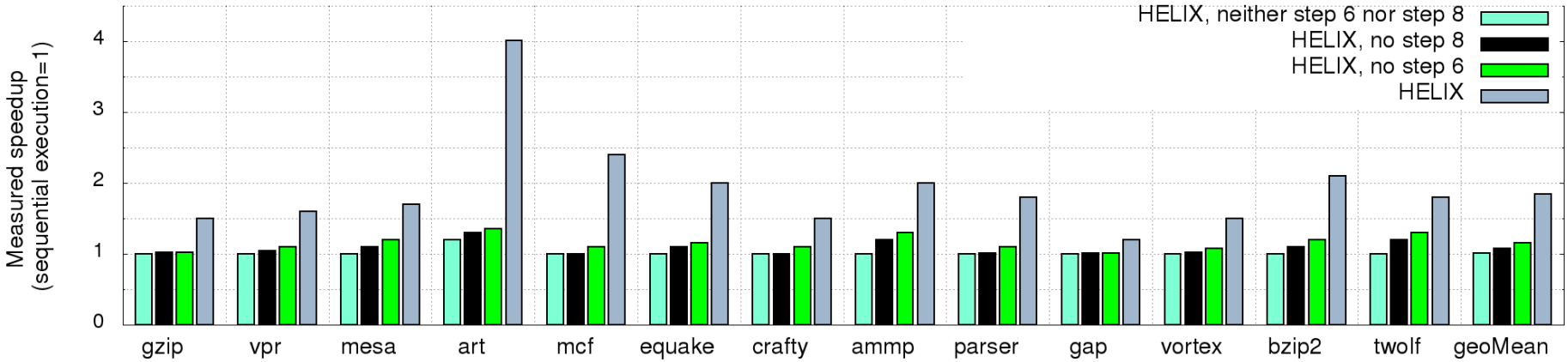

Notice: no slowdown

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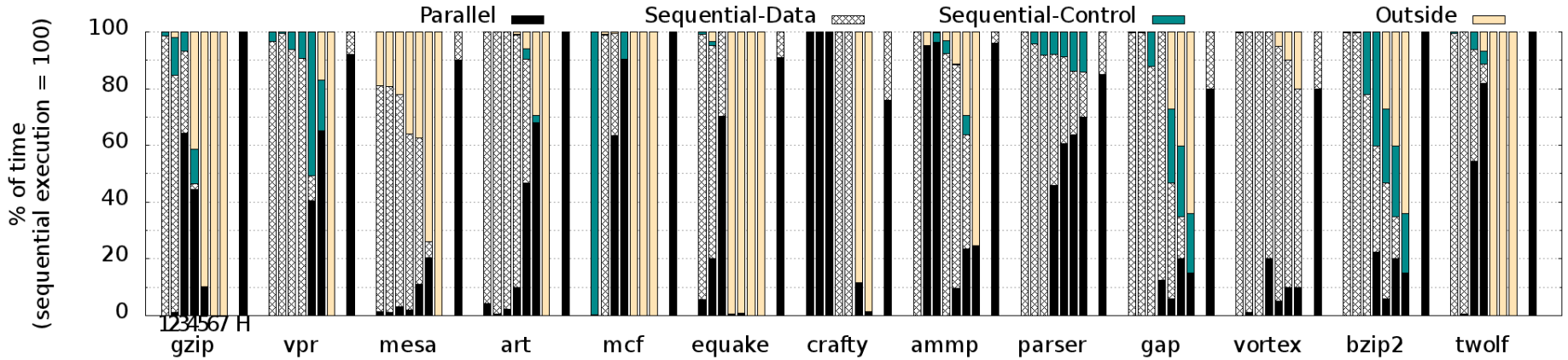

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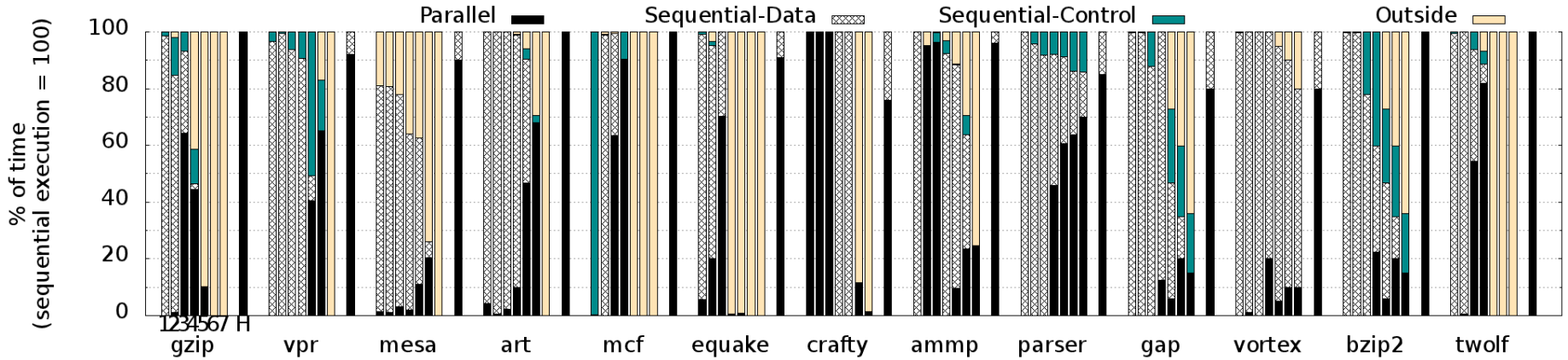

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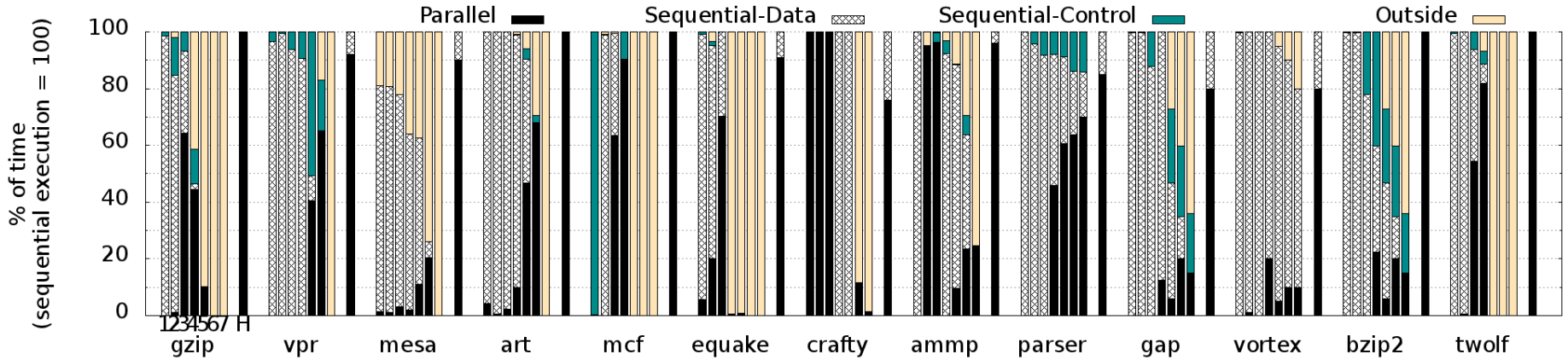

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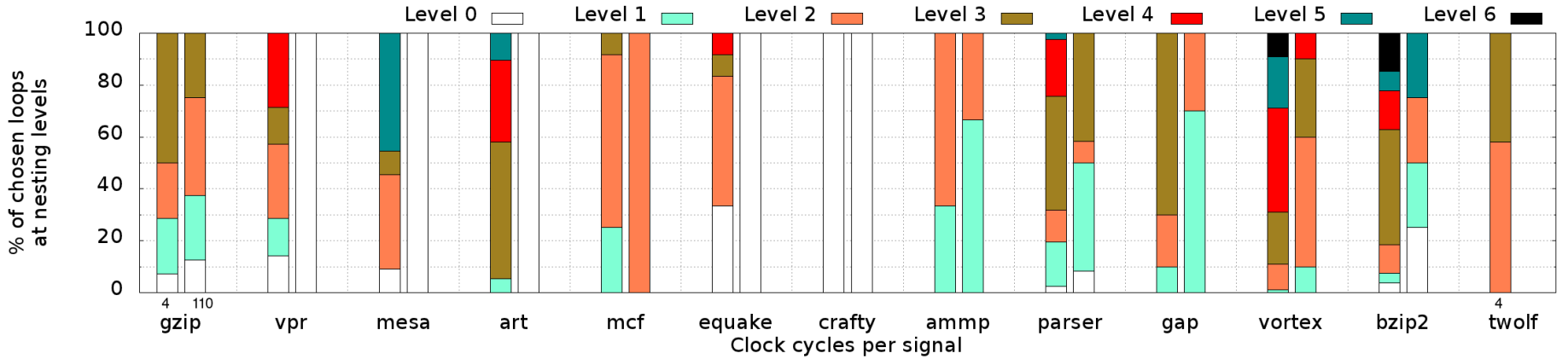

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- What are the limits of HELIX?

References

Websites

- HELIX
  - http://helix.eecs.harvard.edu
- ILDJIT
  - http://ildjit.sourceforge.net

Email

- xan@eecs.harvard.edu

Thanks for your attention!