The HELIX Project: Overview and Directions

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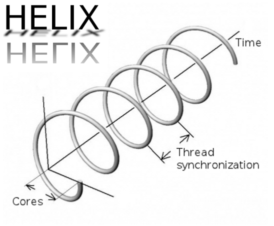
Gu-Yeon Wei, David Brooks

HARVARD
School of Engineering and Applied Sciences



Summary

- Motivation
- The HELIX Research Project
- HELIX on commodity processors
- Adaptive HELIX

Project Goal

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Making the extraction of thread-level parallelism mainstream

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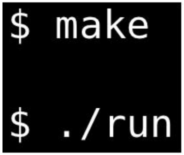

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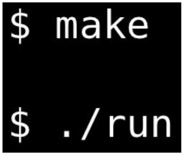

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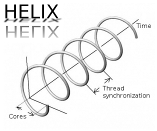

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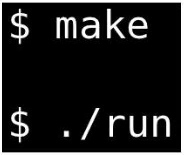

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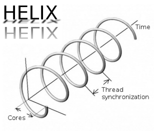

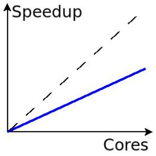

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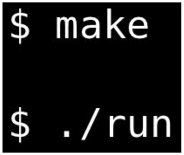

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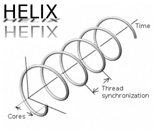

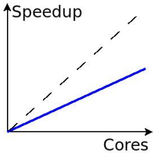

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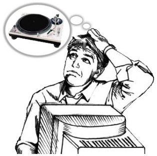

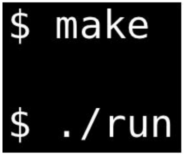

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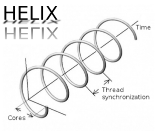

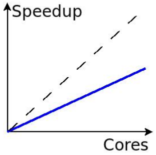

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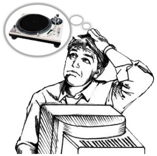

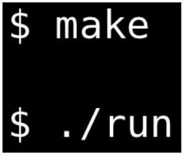

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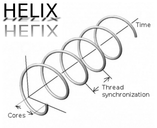

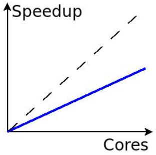

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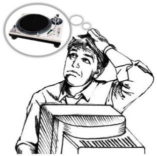

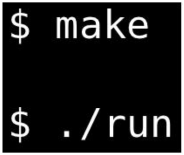

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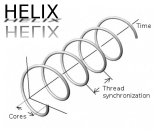

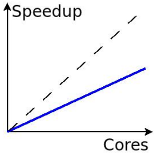

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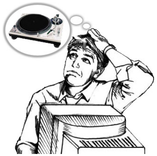
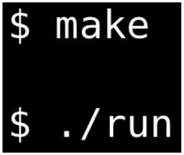

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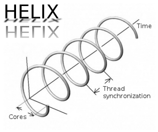

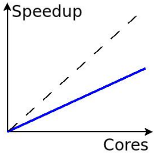

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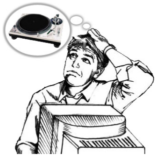

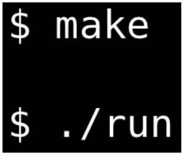

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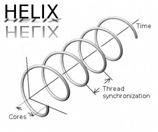

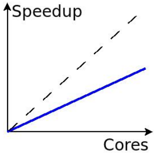

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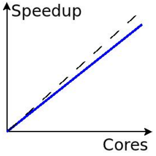

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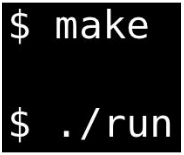

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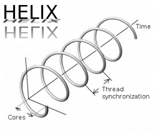

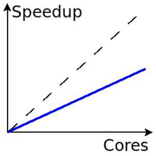

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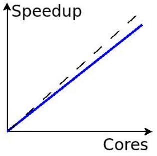

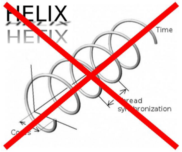

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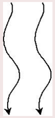
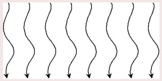

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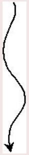
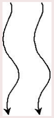
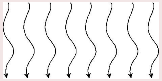
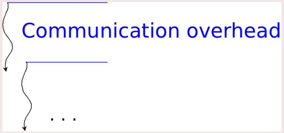




Reduce communication overhead



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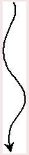

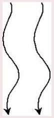

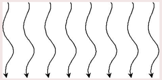

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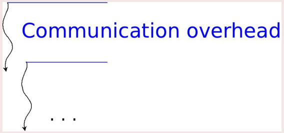

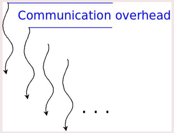

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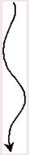
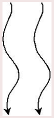
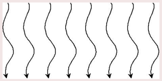

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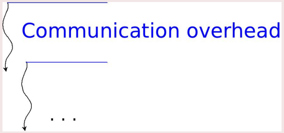

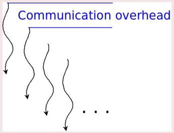

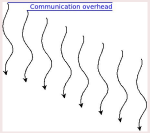

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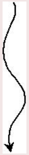
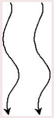
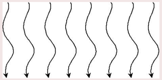

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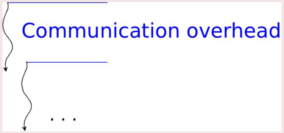

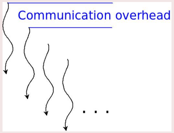

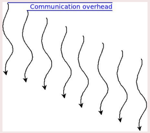

Parallelism $\Leftrightarrow$ *communication*

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Automatic approaches target *loops*

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- General rule:
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- Our analysis:

Covering $\geq$ 98% of program by selecting loops properly is possible

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Main automatic approaches proposed:

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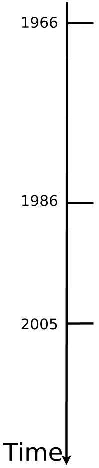

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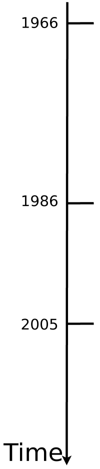

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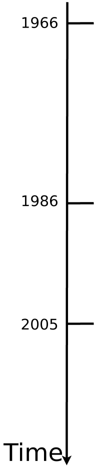

DOALL

Speedup increases with number of cores

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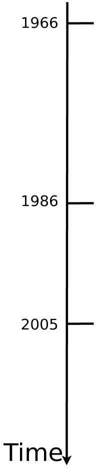

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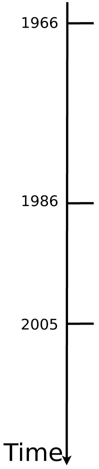

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Is there a way to achieve all of these?

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HELIX

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General purpose technique

DOACROSS $<$ Stability of speedup $<$ DSWP

Produce speedup predictable enough to avoid slowdown

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HELIX

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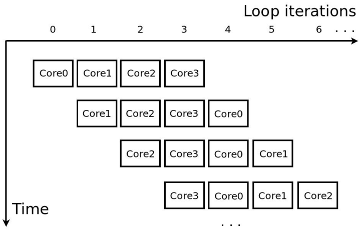

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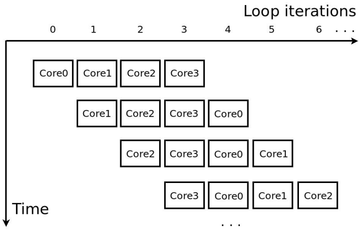

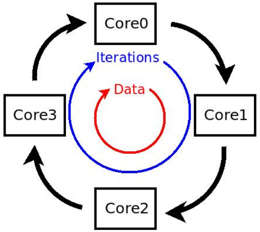

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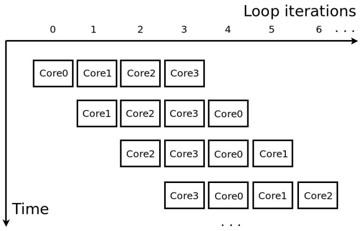

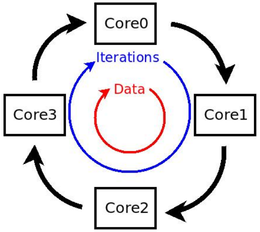

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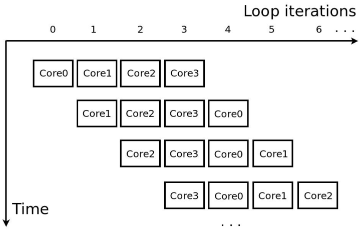
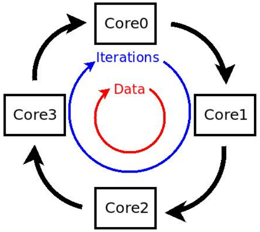
- *Easy* to implement





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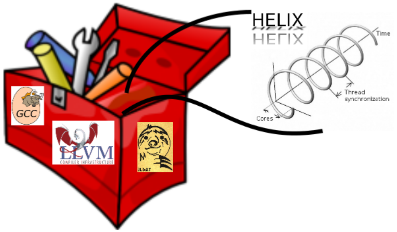

Summary

- Motivation
- The HELIX Research Project
- HELIX on commodity processors
- Adaptive HELIX

A Simple Idea

```
for (...){
    1: a = update(a);
    2: work1(a);
    3: b = update(b);
    4: work2();
}
```

- A simple program

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- Loop-carried data dependences ▨

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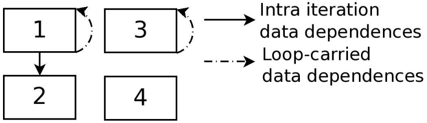
1
2
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Intra iteration data dependences
Loop-carried data dependences

- Idea: exploit independent instructions

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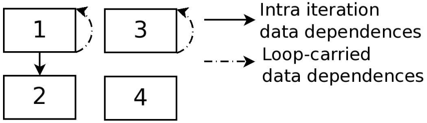
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- Idea: exploit independent instructions *and*

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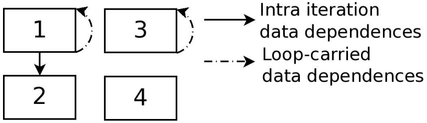
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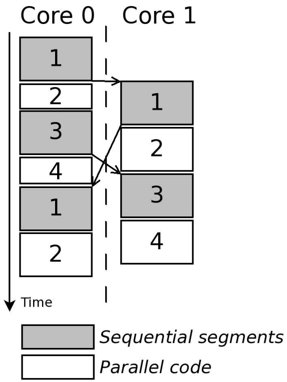

- Idea: exploit independent instructions *and* parallelism among sequential segments

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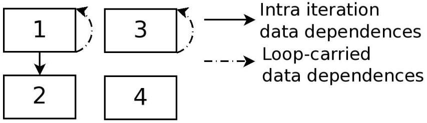

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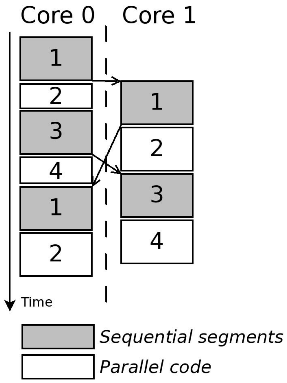

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Problem: amount of synchronization required increases drastically!

Status of HELIX

Prototype

Status of HELIX

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- Target: commodity processors
  - Intel® Core™ i7-980X

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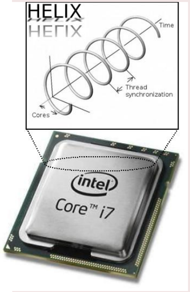

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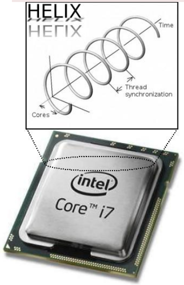

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Status of HELIX

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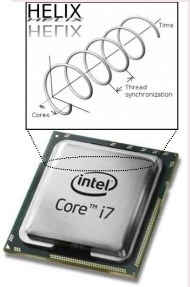

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Status of HELIX

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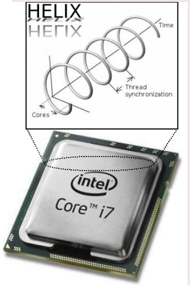

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Status of HELIX

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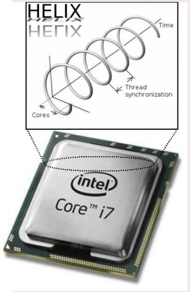

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  - Constrain communication overhead

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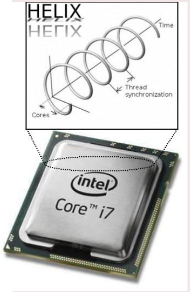

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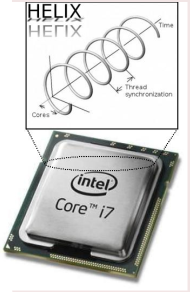

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[CGO 2012, IEEE Micro 2012]

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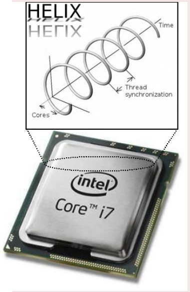

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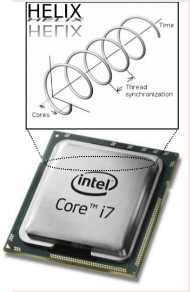

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[CGO 2012, IEEE Micro 2012]

Hardware support

Hardware support

Status of HELIX

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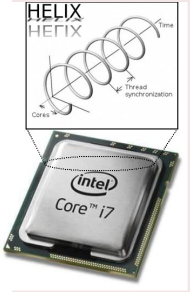

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[CGO 2012, IEEE Micro 2012]

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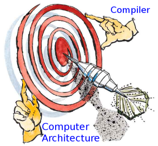

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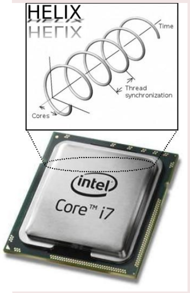

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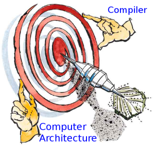
[CGO 2012, IEEE Micro 2012]

Hardware support

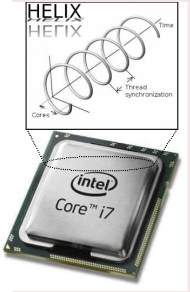


Hardware support

- Push HELIX to the limit

Status of HELIX

Prototype



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[CGO 2012, IEEE Micro 2012]

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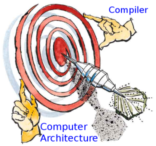
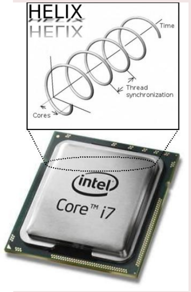


Hardware support

- Push HELIX to the limit
- Minor changes to commodity processors

Status of HELIX

Prototype



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[CGO 2012, IEEE Micro 2012]

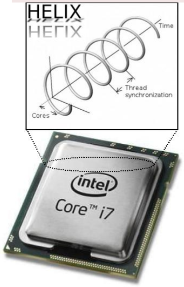
Adaptive HELIX

Hardware support

Adaptive HELIX

Status of HELIX

Prototype



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[CGO 2012, IEEE Micro 2012]

Adaptive HELIX

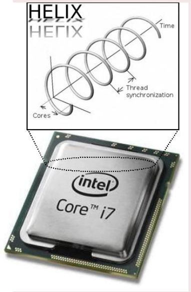
Hardware support

Adaptive HELIX

Adapt code at run time to:

Status of HELIX

Prototype



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[CGO 2012, IEEE Micro 2012]

Adaptive HELIX
Hardware support

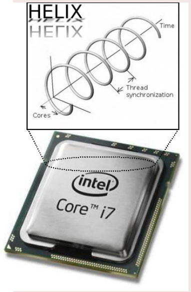
Adaptive HELIX

Adapt code at run time to:

- Parallel behavior

Status of HELIX

Prototype



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[CGO 2012, IEEE Micro 2012]

Adaptive HELIX
Hardware support

Adaptive HELIX

Adapt code at run time to:

- Parallel behavior
- System requirements

Summary

HELIX on Commodity Processors

Overhead

Signalling

Notify threads

Optimizations

Adopted solutions

HELIX on Commodity Processors

Overhead

Signalling

Notify threads

Optimizations

Adopted solutions

- New code analysis to reduce the number of signals to send

HELIX on Commodity Processors

Overhead

Signalling

Notify threads

Optimizations

Adopted solutions

- New code analysis to reduce the number of signals to send
- Code scheduling and use of SMT to reduce the delay per signal

HELIX on Commodity Processors

Overhead

Signalling

Notify threads

Data forwarding

Forward data between threads

Optimizations

Adopted solutions

- New code analysis to reduce the number of signals to send
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HELIX on Commodity Processors

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- Select loops to parallelize

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  - Each loop $\in$ program is analyzed independently
  - These analysis are merged to identify the most profitable loops
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  - Each loop uses all cores decided at compile time

HELIX on Commodity Processors: Evaluation

Platform

- Intel$^{®}$ Core$^{\mathrm{TM}}$ i7-980X with six cores
  - Each operating at 3.33 GHz, with Turbo Boost disabled
- Three cache levels
  - The first two, 32KB and 256KB, are private to each core
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Benchmarks

C benchmarks from SPEC CPU2000

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Compiler

- HELIX has been implemented $\in$ static compiler ILDJIT

Speedup Obtained on a Real System

Overall program speedup

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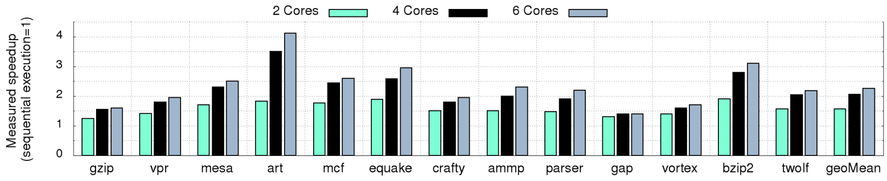

Notice: no slowdown

Summary

- Motivation
- The HELIX Research Project
- HELIX on commodity processors
- Adaptive HELIX

Adaptive HELIX

- Code produced for N cores

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- The number of cores changes to M at run time
    - Performance
    - Multi-programs scenario

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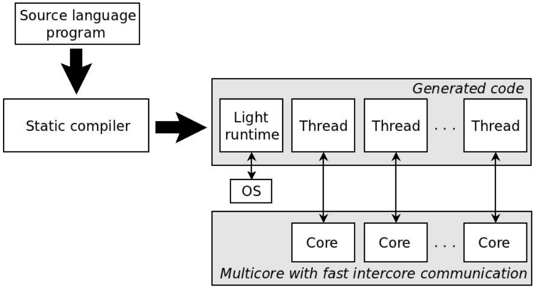

Adaptive HELIX: Cost

What is the cost of adapting the produced binary?

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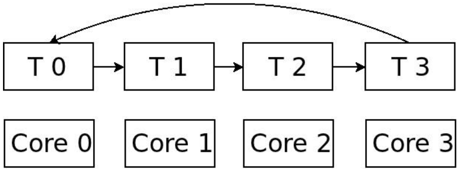

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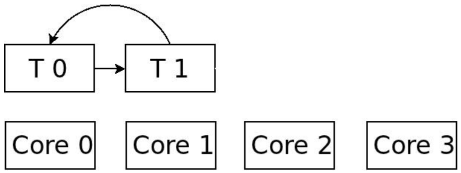

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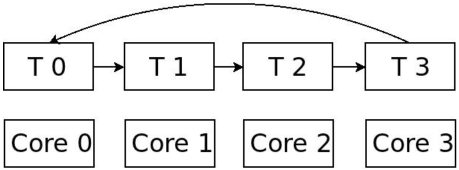

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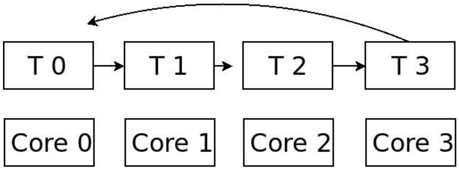

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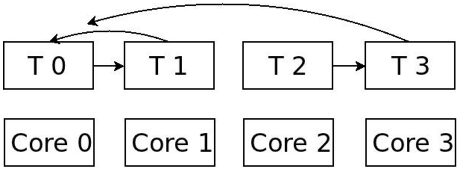

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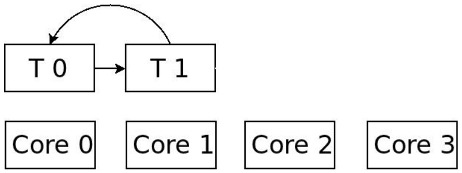

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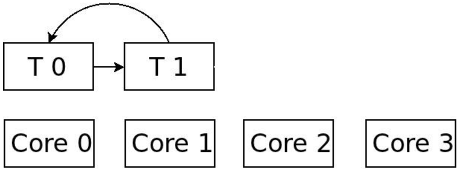

- Few store instructions

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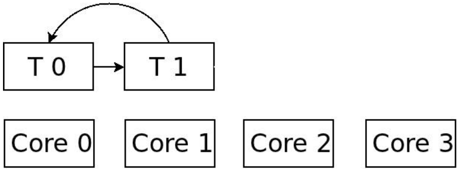

- Few store instructions
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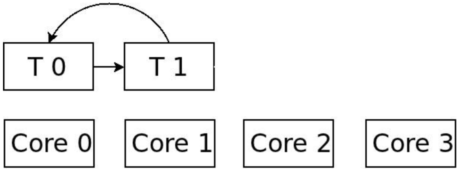

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- Thread management
  - Thread pool

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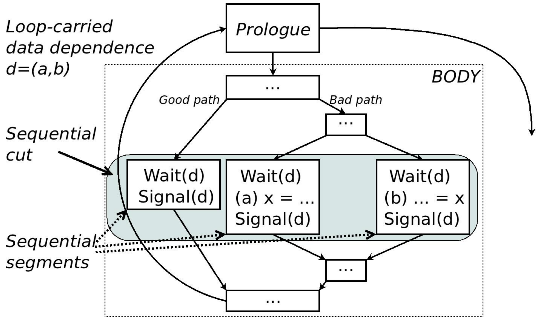
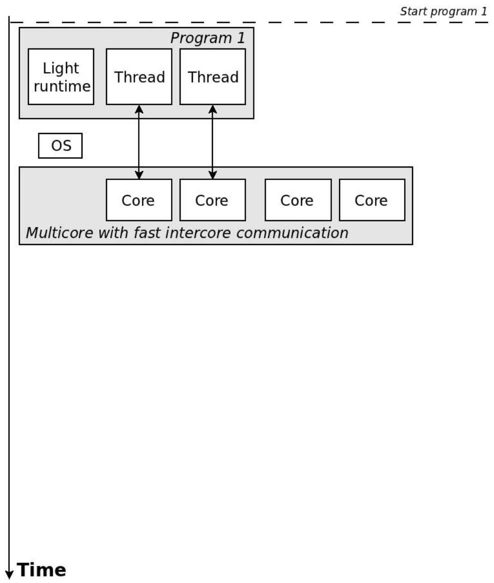
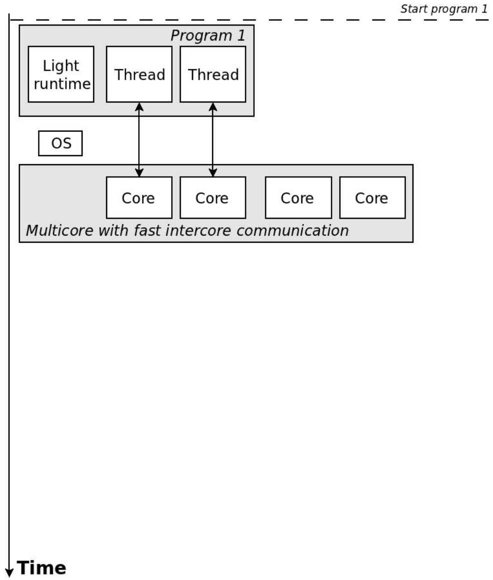

Loop-carried data dependence d=(a,b)
Prologue
BODY
...
Good path
Bad path
...
Sequential cut
Wait(d) Signal(d)
Wait(d) (a) x = ... Signal(d)
Wait(d) (b) ... = x Signal(d)
Sequential segments
...
...

Adaptive HELIX: Performance (2)



- Program 1 has been parallelized for 2 cores

Adaptive HELIX: Performance (2)



- Program 1 has been parallelized for 2 cores
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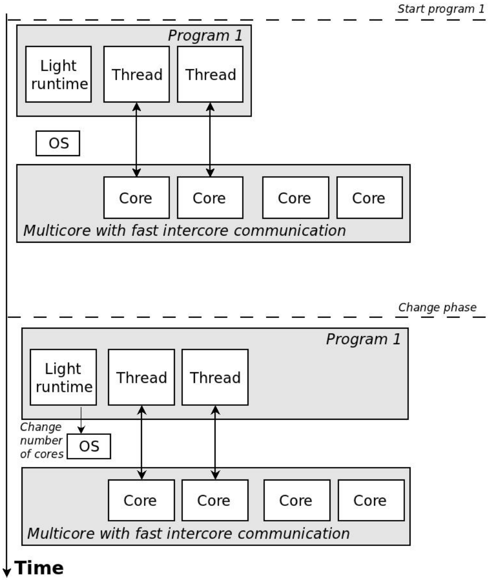

- Program 1 has been parallelized for 2 cores
- The program changes execution phase
- Light runtime starts the interaction with OS

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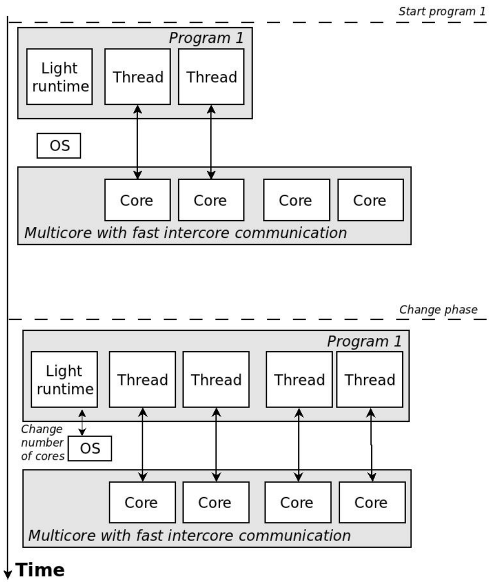

- Program 1 has been parallelized for 2 cores
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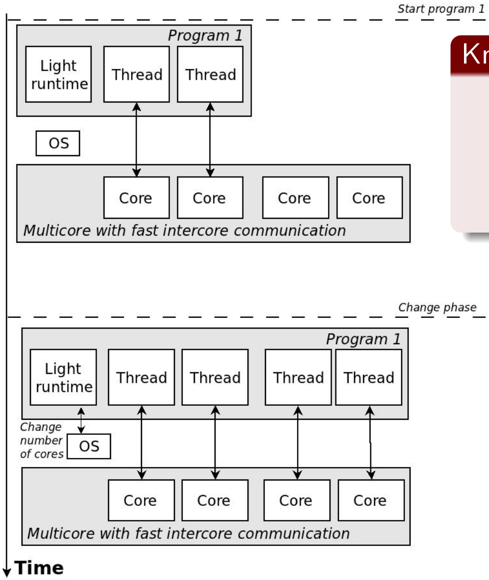

Knowledge

- Program parallelism: *Light runtime*
- Resources available: *OS*

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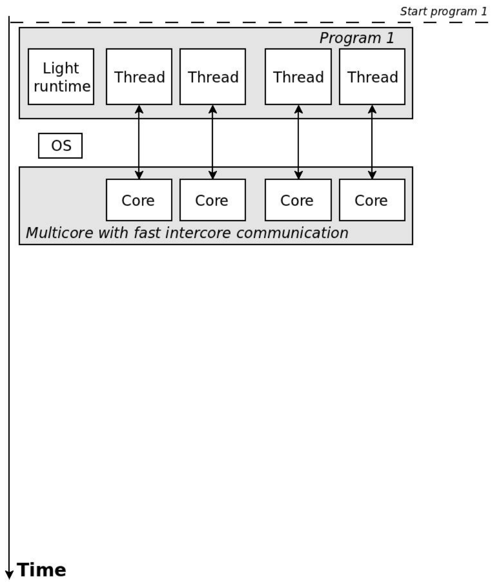
Adaptive HELIX: Multi-programs



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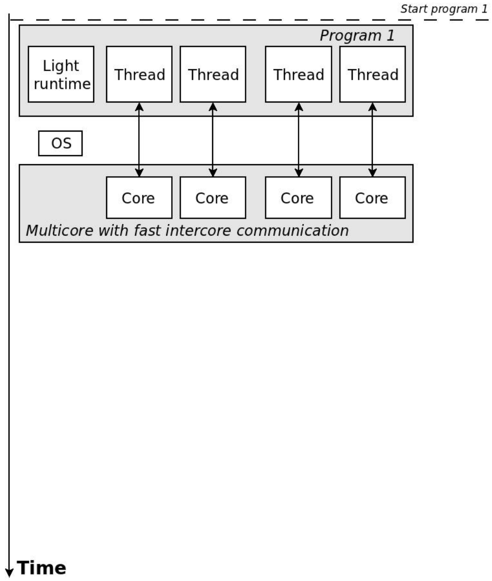

- Program 1 has been parallelized for 4 cores
- Program 2 starts running

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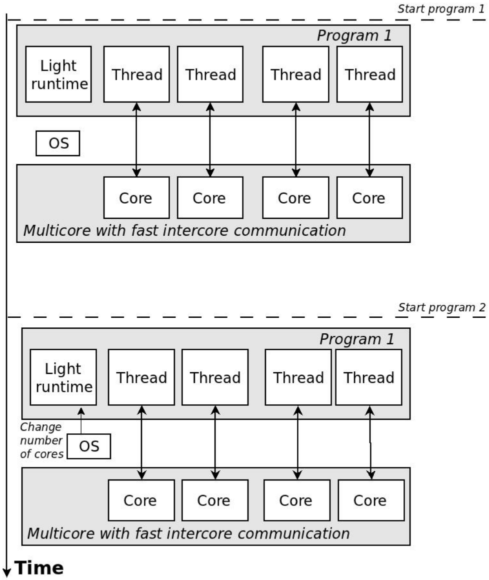

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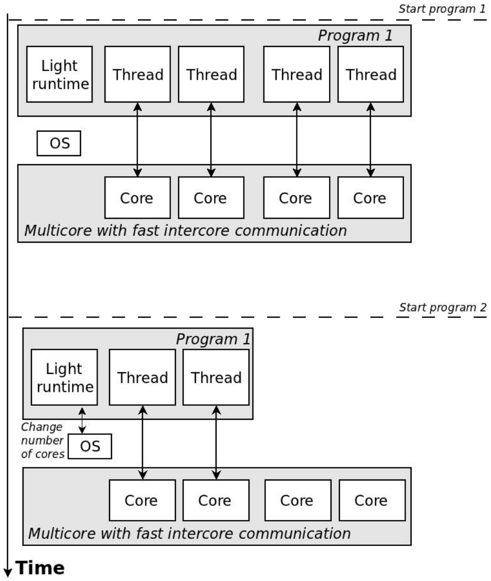

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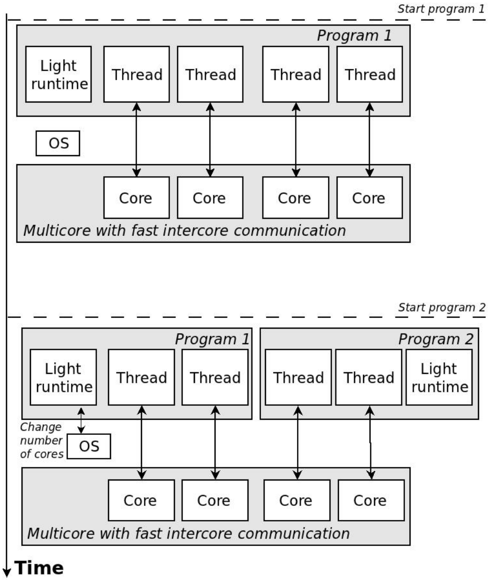

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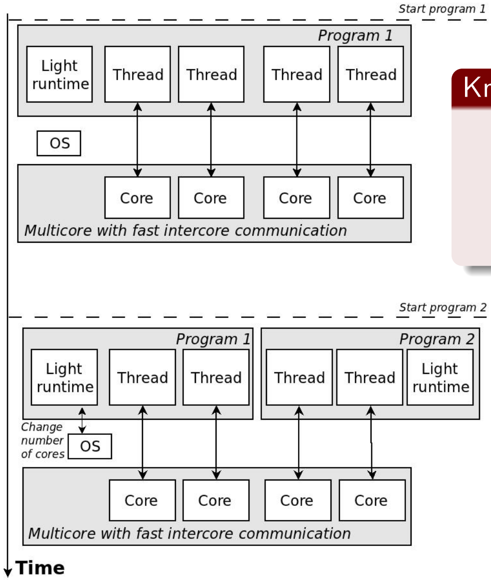

Knowledge

- How to adapt the code: *Light runtime*
- Running programs: *OS*

- Program 1 has been parallelized for 4 cores
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- Program 1 reduces the cores

Conclusion

HELIX: a new general purpose technique to extract parallelism

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- Significant speedups can be achieved on current hardware
    - Hardware not designed for this type of execution
    - Slowdowns are always avoided
- HELIX is able to run both independent and most of dependent code in parallel
- The HELIX code is adapted at run time
    - for performance
    - to handle multiple programs

Light runtime and OS extension is required

Team

References

Websites

- HELIX
  - http://helix.eecs.harvard.edu
  - http://twitter.com/#!/Helix_project
- ILDJIT
  - http://ildjit.sourceforge.net

Email

- xan@eecs.harvard.edu

Thanks for your attention!